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VERTICAL CAVITY LASER JOINT STUDY PROGRAM WITH ROME LABORATORY

Cornell University

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1. ABSTRACT

A program to jointly study vertical-cavity surface emitting lasers (VCSEL) for high speed vertical optical interconnects (VOI) has been conducted under an ES&E between Rome Laboratories and Cornell University. Lasers were designed, grown and fabricated at Cornell University. A VCSEL measurement laboratory previously designed and built under an ES&E was utilized at Rome Laboratory. High quality VCSEL material was grown and VCSEL lasers were fabricated on a 4x4 array for compatility with Rome optical interconnect demonstration programs.

A major effort was development of diamond heat sink mounting of the VCSELs for heat removal. Tasks that were conducted towards successfully meeting this goal included development of solder technology, epitaxial diamond processing, high speed transmission line fabrication and evaluation, and development of flip-chip mounting processes using the flip-chip bonder at Rome Laboratories.

This report includes all details of device fabrication, flip-chip package development and application, and the results of successful demonstration of flip-chip VCSEL arrays.

This report addresses the design, growth, fabrication, and characterization of vertical cavity surface emitting lasers (VCSELs) as well as the fabrication of chemical vapor deposited (CVD) diamond heat sinks and the process of bonding the devices onto the heat sinks.

The growth of VCSELs was built upon previous experience with growing high speed in-plane lasers and used literature guidance to design a gain offset VCSEL with strained 50Å $In_{.3}Ga_{.7}As$ quantum wells that emitted at approximately 1 μm wavelength. To fine tune the growth parameters, an in-line system that used computer modeling and optical reflectometry was developed and demonstrated to produce the first reproducible, continuously graded Bragg mirror VCSELs by MBE without in-situ corrections. Sinusoidal grading over 200Å was used at the $Al_{.9}Ga_{.1}As/Al_{.1}Ga_{.9}As$ interfaces. While this was not the optimum grading scheme, as seen in the high (~3.8 V) threshold voltage of these devices, the unknowns in the continuous grading of MBE effusion cells may make fine-tuning the mirror stack resistivity a difficult challenge.

The work on flip chip bonding these devices onto CVD diamond heat sinks started with the design of coplanar waveguides (CPW) and their microwave characterization up to 40 GHz. The CPW on diamond showed a very low loss of .24dB/cm at 30GHz. Indium was chosen as the solder to attach the completed VCSELs to the end of the CPW and was evaporated in a dedicated evaporator that was designed and built during this project. Although the bonding was very successful, Au-In interactions during the solder evaporation required excessively high temperatures to make reliable bonds. Initial studies on a chrome diffusion barrier were done and, although not used with the devices in this work, showed promise for the next iteration of bonding studies.

The fabricated VCSELs lased in a continuous wave at room temperature and had similar output power and wavelength both bonded and unbonded. Single mode behavior (>40 dB SMRR) was exhibited on all devices. Thresholds on devices bonded to diamond were slightly higher than those for unbonded devices while the threshold wavelength remained the same. This result shows that the thermal resistance of the devices had been reduced and that more current was necessary to heat the device to the point at which there was optimum overlap between the gain spectrum and the cavity mode.

Fundamentals of material growth

All of the wafers used in this study were grown on a Varian Gen II MBE system designed for 2" substrates, using solid-source evaporants. Computer control of the growth was implemented by a program written and updated at Cornell over the past 12 years. The first few VCSEL growths and all calibration runs were done on pieces of 3" semi-insulating (SI) GaAs wafers that had undergone a thorough solvent cleaning and then a one minute etch in a H_2SO_4:H_2O_2:H_2O (5:1:1) solution followed by a thorough rinse in de-ionized (DI) water. The wafers were mounted onto molybdenum blocks using indium solder and loaded into the MBE machine. The last few VCSEL runs, which are the ones that exhibited continuous wave (CW) operation, were grown on 2" SI epi-ready substrates ((100) 2±0.25° off towards the nearest <110> from Acrotec) which were mounted to molybdenum blocks without any chemical preparation. Epi-ready substrates were used for the sake of convenience and because the machine time charged to a VCSEL (12-15 hours @ $330/hour) justified the extra cost of epi-ready wafers. No significant improvement in defect density was noted and the difference in device performance was attributed to a better design, rather than better substrate conditions. Growth rates for all materials were determined by intensity oscillations in the reflection high energy electron diffraction (RHEED)[1,2,3] patterns.

Growth of GaAs

The growth of GaAs has become very standardized in the field of MBE. The block and wafer are initially outgassed (near 300°C) in a preparation chamber to remove much of the adsorbed atmospheric gasses before moving it into the growth chamber. After they are transferred to the growth chamber, they are heated to 500°C under an As flux. They are then slowly warmed to ~570°C at which point the thin surface oxide (from the final water rinse) desorbs from the surface. The temperature is then raised 20°C for about one minute and then returned to the temperature at which the oxide desorbed from the surface. Growth of undoped GaAs at a growth rate of 1 μm/hr is then initiated. A strong 2×4 surface reconstruction was observed after desorption for all of the wafers that underwent chemical preparation, but on the above-mentioned epi-ready substrates, the surface did not show good 2×4 reconstruction until a few monolayers of GaAs were grown. Because of the non-uniformities between different molybdenum blocks and

inconsistencies in the indium mounting technique, the congruent sublimation temperature (T_{CS}) of GaAs (640°C) was determined for each wafer by slowly raising the temperature and noting the temperature at which the surface reconstruction pattern changed from 2×4 to 4×2 in the absence of As flux. The current set of blocks typically read between 620 and 650°C on the thermocouple when the wafer surface is 640°C.

In the growth of GaAs, almost all groups use a substrate temperature between 580 and 600° C and a beam equivalent V/III flux ratio of 4-7. This results in growth with an arsenic stabilized surface with a 2×4 reconstruction. A V/III flux ratio near 5 was used for all the 0.5 μm/hr GaAs growth in this report. The As species used was As_4 from solid source As.

Growth of AlGaAs

The growth of good optical quality AlGaAs is necessary for efficient high speed devices. Good optical quality AlGaAs is material with a small number of non-radiative recombination centers. Good optical quality AlGaAs tends to increase the quantum efficiency of the devices and translates into high speed through reduced threshold currents, high output powers at low drive currents, and thus less resistive heating of the devices. In standard in-plane lasers, the optical fields extend thousands of Angstroms into the clad regions, which are typically AlGaAs with 70 to 80% Al content. Large numbers of non-radiative centers in this part of the device will degrade device performance.

Like in-plane lasers, the strong optical fields in a VCSEL extend about 1 μm into the Bragg stacks. In order to achieve the highest reflectivity with the fewest number of Bragg layers, the largest change in refractive index between the layers is desired. In the ideal situation, pairs of GaAs and AlAs layers would form the Bragg stack. For reasons to be related later in this section, this is not electrically practical, but large changes in the Al content of the alloys is still desired. The aluminum content of the Bragg pairs is in this work varied from a low of 10% to a maximum of 90%. Thus, good optical quality high Al content material is required in a VCSEL as well.

The growth of high optical quality, high aluminum content alloys is not straightforward, but previous experience with the growth of in-plane lasers was a good starting point for the growth

of the Bragg mirrors. Experience with the growth of the cladding region of in-plane lasers has shown that $Al_{.7}Ga_{.3}As$ grown at a substrate temperature of 710° C with only very small overpressures of arsenic produces devices with very high efficiencies. The appropriate As flux is determined by growing $Al_{.7}Ga_{.3}As$ at 710° C and adjusting the flux so that 3×1 reconstruction is observed in the RHEED patterns. This rate corresponds to an As flux that would be adequate to grow GaAs at 0.7 μm/hr[4].

The $Al_{.7}Ga_{.3}As$ for the optical guide of an in-plane laser is grown with a GaAs growth rate of 0.5 μm/hr and an AlAs growth rate of 1.05 μm/hr. This gives a combined growth rate of 1.55 μm/hr and an Al mole fraction of 67.7%. But at elevated growth temperatures (>640°C) there is a non-negligible flux of Ga atoms leaving the growth surface[5,6]. The assumed GaAs growth rate is 0.45μm and the resulting mole fraction is nearer to 70%. For in-plane lasers, this uncertainty in mole fraction is not critical, as long as it is reproducible, but for VCSELs, the loss of gallium from the growth surface while growing high aluminum content alloys at high temperatures is a difficult to calibrate uncertainty in the optical thickness of the Bragg stacks.

For the VCSEL growth, a compromise was made between crystal quality and mole fraction control. For the entire mirror growth, the substrate was held at 620° C to hopefully eliminate Ga desorption, while using a slightly elevated substrate temperature to improve the surface mobility of Al atoms. In a future study, the substrate temperature could also be increased as the Al mole fraction was increased, leading to one more uncertainty in the growth of the mirrors, but possibly improving the overall quality of the devices.

Growth of InGaAs

Analogous to the problem of desorption of Ga from the growth surface at temperatures above 640° C, indium starts to desorb from the growth surface at temperatures above about 520° C[7]. It has been found that the best optical quality InGaAs is grown just below this temperature[8]. For this work, the $In_{.3}Ga_{.7}As$ quantum wells were grown at 500° C with a GaAs growth rate of 0.5 μm/hr and an InAs growth rate of 0.2143 μm/hr. This low substrate temperature meant that growth interruptions were necessary before and after the quantum wells to change substrate temperatures. $Al_{.15}Ga_{.85}As$, grown at a substrate temperature of 620° C, was used as the barrier

material in the cavity. A 2.5 minute growth interruption was necessary to drop the substrate temperature from 620° C to just below 500° C, including recovery from a 15-20 degree undershoot. The 50 Å quantum well was grown in just over 25 seconds and, while still at 500° C, 10 Å of $Al_{.15}Ga_{.85}As$ was grown to prevent In desorption from the QW during the second, 2 minute, growth interruption. During the interruption, the substrate temperature was raised to 620° C. At the end of the 2 minutes, growth of $Al_{.15}Ga_{.85}As$ was resumed. This sequence was repeated for each of the three quantum wells used in the VCSEL design. (This style of QW growth sequence has been used by our group for several years with much success.) This active region, was chosen because this same structure has been grown in our edge-emitting lasers and its photoluminescence emission and laser emission properties are well characterized.

Bragg mirrors

Bragg mirrors are pairs of quarter-wavelength thicknesses of materials with alternating high and low refractive indices. These materials can be oxides (SiO, TiO, MgO), nitrides (SiN, TiN), or semiconductors (Si, Ge, GaAs, AlGaAs). Larger differences between the refractive indices of the two materials corresponds to smaller numbers of mirror pairs that will be necessary to produce a given reflectivity. Also, larger differences in refractive indices result in wider mirror stopbands. Unfortunately, for the GaAs/AlGaAs system, the change in refractive index is very small ($\Delta n = 0.6$ between GaAs and AlAs at a wavelength of 1 μm) so a large number of mirror pairs is required and the stopband is quite narrow (~40 nm) for these mirrors. To obtain a 99.9% power reflection (simulated) from an AlAs/GaAs mirror at a wavelength of 1 μm, 19 pairs are required. With each pair having a thickness of 1567Å, the mirror is 2.97 μm thick. To assist in the design of Bragg stacks and VCSELs, a program called REFLECT was written under an ONR AASERT grant to model the reflection spectrum of an arbitrary layer stack.

Design of a VCSEL structure

Many papers describing the design of VCSELs have been presented in the literature[9,10,11,12,13,14,15,16]. These were used as guidelines for the theory of how to produce VCSELs while the in-house technology for the growth and characterization of the Bragg mirrors was developed.

To grow a VCSEL, there are several parameters which need to be controlled to within a few nanometers: (1) the transition energy of the quantum well and thus the spectral position of the gain spectrum, (2) the length of the cavity and thus the emission wavelength, and (3) the center wavelength of the Bragg mirrors. For a VCSEL with a planned emission wavelength of 1 μm, an error in growth rate of 1% results in a wavelength shift of 10 nm in the Bragg mirrors. It was decided that control of all Bragg layer thicknesses to better than 0.5% (5 nm error) was necessary.

It was learned in the early 1990's that these three parameters should not all be at the same wavelength[17]. The inevitable heating of the devices would very quickly detune the structure. Thus, the temperature sensitivities of the different parts of the structure were investigated and it was found that the QW transition should be blue-shifted from the cavity wavelength by about 0.25 nm/°C of temperature rise during operation of the device. At a supposed rise in junction temperature of 100° C[17], this leads to a 25 nm designed offset. This offset is actually dependent upon the design of each particular wafer, device size, and fabrication technique.

The initial design parameter is the emission wavelength of the quantum wells because the cavity length and Bragg mirror stop band will be referenced to this wavelength. The quantum well design is very similar to that of the high speed in-plane lasers grown at Cornell. Three 50 Å $In_{.3}Ga_{.7}As$ quantum wells with $Al_{.15}Ga_{.85}As$ barriers were to be used as the gain medium for these devices. Experience with the critical layer thickness of multiple quantum wells[18,19] determined the center-to-center spacing of the quantum wells to be 190 Å. Photoluminescence results from edge-emitting lasers grown with the same quantum well design showed a transition wavelength of 990 nm. These quantum wells were centered in a one-wavelength-long cavity of $Al_{.15}Ga_{.85}As$ which was designed to be at an optical length of 1000 nm. An offset of 10 nm was chosen because the goal of both the VOI project and the high speed measurements was to make devices which work well while mounted to diamond heat sinks. With these heat sunk devices, there should be less of a change in active region temperature during operation. The difference between the refractive index of GaAs and $In_{.3}Ga_{.7}As$ was not considered when designing the length of the cavity, but their 150Å thickness was included in the length of the cavity. Emission at a wavelength of almost exactly 1 μm was achieved in the fabricated devices, both unbonded and bonded. Because the tuning of the third parameter, cavity length, is achieved

automatically by using the proper growth rates for the Bragg mirror, nothing more will be said about cavity length tuning.

Bragg mirrors consisting of many layers of GaAs/AlGaAs pairs form a very well-behaved optical structure, but unfortunately for VCSELs, it also behaves as a very large series resistance due to its many heterointerfaces. There are many techniques in the literature for reducing the series resistance of a Bragg stack: step-graded interfaces[20], continuously graded interfaces[21],[22], short-period superlattice grades[23], and doping dipoles[24]. These techniques are combined with moderately high doping levels[25] to obtain low series resistances with minimal free carrier absorption. All of the above techniques also need to maintain a high degree of stability over the long growth times of these devices (12-15 hours). It is generally thought that continuously graded mirrors grown by MBE, which changes effusion cell temperatures to change growth rates, are not a reproducible technique. The only previously reported use of continuously graded interfaces in a Bragg mirror (without in-situ tuning) was demonstrated with linear grades in a metalorganic chemical vapor deposition (MOCVD) system, where mass flow controllers are used to change the growth rates[21]. Results from this report show predictable and reproducible Bragg stacks and VCSELs can be made using continuously graded interfaces grown by MBE.

To continuously grade growth rates in an MBE system, the growth rate as a function of cell temperature needs to be known accurately. For growth at a substrate temperature where no desorption is taking place, the growth rate takes the following form:

$$Rate = R_0 \, exp\left(\frac{-E_a}{kT}\right)$$

where T is the effusion cell temperature and k is Boltzman's constant. R_O and E_a are constants which are determined for each cell by calibrating growth rates over about an order of magnitude by RHEED oscillations. This is a standard calibration for the MBE machine and was not done explicitly for this work. This form of the flux equation is used because it relies only upon actual machine calibrations of cell temperature and accurately predicts the behavior of a cell over more than an order of magnitude of growth rates. This information is entered into the computer which then automatically calculates the cell temperature required to produce a given growth rate. If the changes in growth rates are small enough and happen often enough, then the cell can, in effect, be continuously graded in an arbitrary way. In reality, the thermal mass of the cell and heat loading of the LN_2 panels need to be considered and arbitrary grades are not possible.

A growth rate was chosen so that the grading could be controlled over a distance of 200 Å, approximately 1/8 of the length of the Bragg pair. Experimentally, it was determined that these grades could be achieved with realistic temperature lag and overshoot by growing at a constant rate of 0.5 μm/hr. At this growth rate, the 200 Å grade from $Al_{.1}Ga_{.9}As$ (AlAs 0.05 μm/hr; GaAs 0.45 μm/hr) to $Al_{.9}Ga_{.1}As$ (AlAs 0.45 μm/hr; GaAs 0.05 μm/hr) was performed in 2.4 minutes in 20 steps. More steps might have resulted in a more accurate mirror, but programming (the total number of steps) and machine communications limitations (time to execute an instruction) limited the number of steps to 20. However, it was found that this was not the best design of a grade. The temperature changes at the beginning of the grades were too big for the thermal inertia of the cells, and there was some overshoot at the ends. A better design for the grading sequence was sinusoidal. The temperature changes at the beginning of the grade start small and gradually increase, while the middle is more steeply sloped, and the gradually decreasing step sizes near the end of the grades help to minimize overshoot. The ideal structure for minimizing accumulation of carriers at the heterointerfaces is a parabolically graded structure[26], but the small differences between the two designs were expected to be lost in the noise of the stepsize and overshoot errors of the cells. Sinusoidal grades were used in all calibration and VCSEL growths.

Growth and optical tuning of Bragg mirrors and VCSELs

A systematic technique for tuning the growth of a Bragg mirror and the cavity length of the VCSEL is required because of the many sources of error that occur between the initial design and the grown wafer. The first source of error is the published $Al_xGa_{1-x}As$ refractive index data, independent of the source of the data. Although the data is good on a relative scale, absolute errors on the order of a few percent are to be expected, especially after extrapolation for different alloy contents at different wavelengths. A second source of error occurs when calibrating growth rates with RHEED oscillations[27,28,29]. Knudsen cells in an MBE system have flux transients which arise from the fact that heat from the cell is reflected back towards the charge while the shutter is closed. The temperature, and thus the flux, of the cell just after opening the shutter is higher than a few seconds later. Because RHEED oscillation measurements are made in the first few seconds after opening the shutter, the growth rate can easily be overestimated by a few percent. The third error comes about because of the grading

scheme used in this project. The actual shape, and thus the optical length of the graded region is unknown, so modeling a sinusoidal transition is only an approximation. Because of all these uncertainties, another calibration technique with an accuracy and reproducibility greater than 0.5% is necessary. Optical techniques are the obvious choice.

Optical measurements typically have accuracies much better than the resolution necessary for this project. Thus, a reflectometer was built with the requirements of fast turnaround and the ability to accept arbitrary size samples (from small test pieces up to 2" wafers). In order to obtain a tunable, quasi-monochromatic light source, the output from a high power fiber illuminator was passed through a small monochromator with a voltage output that corresponds to the wavelength of light at the exit slit. With the slits almost totally closed, a light source with a bandwidth of about 1 nm was obtained. The quasi-monochromatic light from the exit slits of the monochromator was focused into one branch of a bifurcated fiber bundle. The double-bunch end of the bundle was mounted, upward looking, in a Plexiglas® table and the sample was placed face-down onto the table above the end of the bundle (which was recessed enough from the top surface of the table that reflected light was efficiently coupled back into the fibers from the other half-branch). The reflected light in the second branch of the fiber bundle was directed onto a packaged 5 mm Ge photodetector that was unbiased. The light beam was chopped at a few hundred Hz and the collected signal was measured using a lock-in amplifier without any amplification of the signal. A schematic of the apparatus is shown in Figure 2.1.

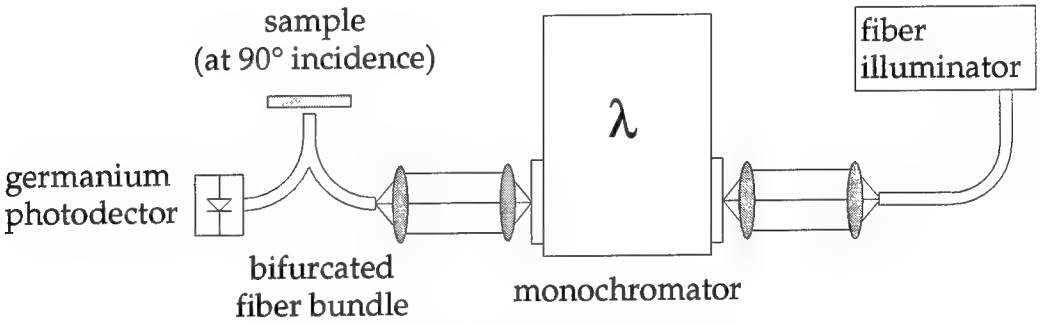

Figure 2.1 : Reflectometer schematic

A computer program written in LabView® and an ADC board were used to collect data for wavelength and reflected power. A reflection spectrum could be measured in about 2 minutes using this system. Because of the very non-linear response of the photodetector, lamp, and

optical elements, and the difficulty in determining an accurate calibration sample, absolute reflectivities were not measured, but the wavelength accuracy of the system was better than 1 nm due to daily calibrations using the 1013.9 nm line of a low-pressure Hg lamp. Reproducibility of measurements when the sample was removed and replaced on the stage was higher than the accuracy of the measurement. With an accurate and reproducible measurement technique in place, REFLECT and a test sample could be used to tune the growth parameters.

The ability to model the effects of independent changes in the Ga, Al, and In growth rates was a feature that was built into REFLECT. For example, the program gives the resulting reflection spectrum if the Ga growth rate were 2% too low by executing the command 'RATE Ga 0.98' in the second section of the input file. The effect of variations in both GaAs and AlAs growth rates on the reflection spectrum are easily be determined without the need for the user to modify any mole fraction information in the input file. The modifications are made automatically when the .TFILE is written. A test structure that was independently sensitive to GaAs and AlAs growth rates was required.

Such a structure has been presented in an application note for a small company that markets an MBE reflectometer and modeling software[30]. The structure consists of a Bragg mirror of AlAs and GaAs, but with an extra 1/4 wavelength layer of GaAs on top of the stack. Without the extra layer, a standard Bragg mirror structure is formed, but the extra layer of high refractive index material modifies the reflectivity by putting a notch into the stopband of the mirror. The top layer thickness, and thus the GaAs growth rate, uniquely determines the position of the notch while the position of the first nulls of the structure are used to determine the AlAs growth rate. To tune the VCSELs, a ten-period, graded, doped Bragg mirror, identical to the design to be used in the VCSEL was used for the Bragg mirror of the test structure while a quarter wavelength section of $Al_{.1}Ga_{.9}As$ was used as the extra layer. To first order, the motion of the dips in the reflection spectra behaved as expected, but it was necessary to simulate the relationship between the shift in the nulls and the change in growth rates. The wafer design was given the designation GRCAL for growth rate calibration wafer.

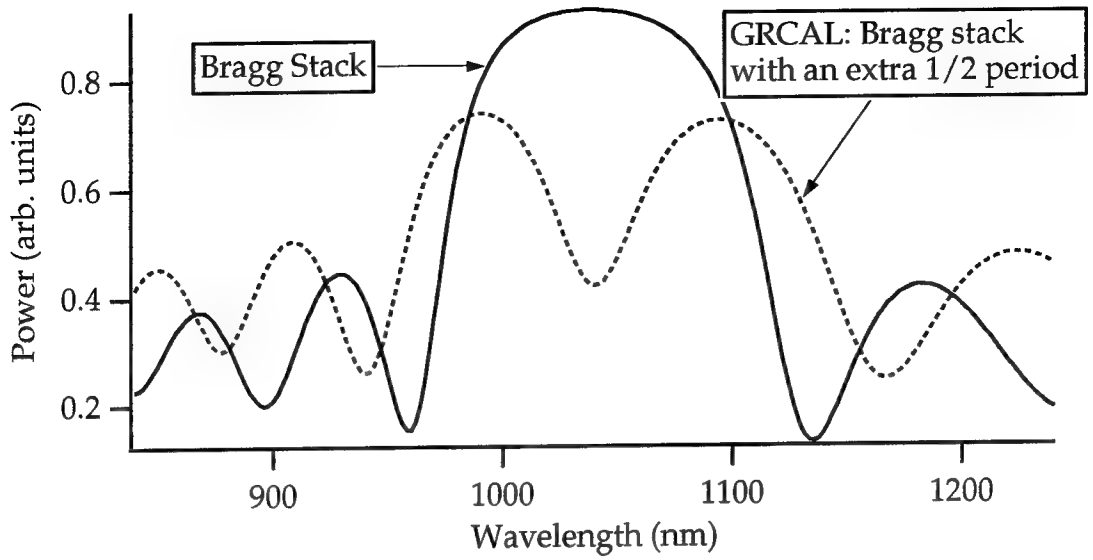

Figure 2.2: Simulated reflection spectrum of GRCAL

Before growing the wafer, REFLECT was run for all of the permutations of errors in GaAs and AlAs growth rates from +3% to -3%, in 1% increments. The test wafer was then grown and the reflection spectrum measured. By comparing the spectrum to the sets of simulated data, the appropriate percentage changes in growth rate could be determined and another layer grown. Typically, a large change (3-5%) in growth rates was necessary after the first calibration layer, but the second layer was typically close enough to the desired wavelengths to justify making the minor adjustments necessary and then growing a real VCSEL.

Measured results of two consecutively grown test samples showed 1 nm reproducibility of the continuously graded mirror structure. By comparing several simulations to the data, the best fit may be obtained. The growth rates can then be modified by the amount of the simulated error. Figure 2.3 shows the complete layer structure used for the VCSEL wafers. It is important to note that all of these thicknesses are off by a few percent and have been tuned to the correct thicknesses using reflectometry. The layers marked with '♦' are for phase-matching and are necessary because the optical middle of the grade is considered to be the interface of the Bragg stack.

The reflection spectrum from four places near the middle of a wafer that showed CW device operation is shown in Figure 2.4. The insert shows an enlarged view of the cavity dip. A

simulation of the whole VCSEL is qualitatively no different from a simulation of the test structure. Modification of the growth rates can also be made between VCSEL growths by using the VCSELs themselves as calibration wafers. The dip in the spectrum showing the spectral position of the cavity is the extra piece of information gained from reflectometry on the real devices. The sharpness of the spike shows the uniformity of the mirror stacks and, through a convolution, the linewidth of the probing beam. A second wafer with a very similar spectrum was grown after this one and also showed CW device operation slightly longer than 1 μm wavelength. Because of a 1-2% non-uniformity in the growth rate across the wafer, reflectometry can be used to determine which parts of the wafers are expected to lase before processing occurs. It is because of this non-uniformity in growth rate that the wafer was designed for 1010 nm. When the center of the wafer has a 1010nm cavity, a large portion of the wafer has a cavity length near 1000 nm.

LAYER	Alloy	Doping/cm^3	h (Å)	% AL	% IN
CAP	GaAs	p+ :4.0E+19	718.94		
CAP ♦	AlGaAs	p :6.0E+18	95.24	0.10	
CAP	AlGaAs	p :6.0E+18	545.34	0.10	
graded	AlGaAs	p :6.0E+18	200	0.9 -> 0.1	
HIGH Al	AlGaAs	p :6.0E+18	628.16	0.90	
graded	AlGaAs	p :6.0E+18	200	0.1 -> 0.9	
LOW Al	AlGaAs	p :6.0E+18	545.34	0.10	
# REPEATS:	20	Total:	31470		
graded	AlGaAs	p :2.0E+18	200	0.9 -> 0.1	
HIGH Al	AlGaAs	p :2.0E+18	628.16	0.90	
HIGH Al ♦	AlGaAs	p :2.0E+18	118.14	0.90	
Barrier	AlGaAs		1262.52	0.15	
QW	InGaAs		50		0.30
Barrier	AlGaAs		140	0.15	
QW	InGaAs		50		0.30
Barrier	AlGaAs		140	0.15	
QW	InGaAs		50		0.30
Barrier	AlGaAs		1262.52	0.15	
HIGH Al ♦	AlGaAs	n :2.0E+18	118.14	0.90	
HIGH Al	AlGaAs	n :2.0E+18	628.16	0.90	
graded	AlGaAs	n :2.0E+18	200	0.1 -> 0.9	
LOW Al	AlGaAs	n :3.0E+18	545.34	0.10	

graded	AlGaAs	n :3.0E+18	200	0.9 -> 0.1	
HIGH Al	AlGaAs	n :3.0E+18	628.16	0.90	
graded	AlGaAs	n :3.0E+18	200	0.1 -> 0.9	
# REPEATS:	20	Total:	31470		
Doped buffer	GaAs	n+ :4.0E+18	>5000		

Figure 2.3: Layer thickness diagram for a VCSEL

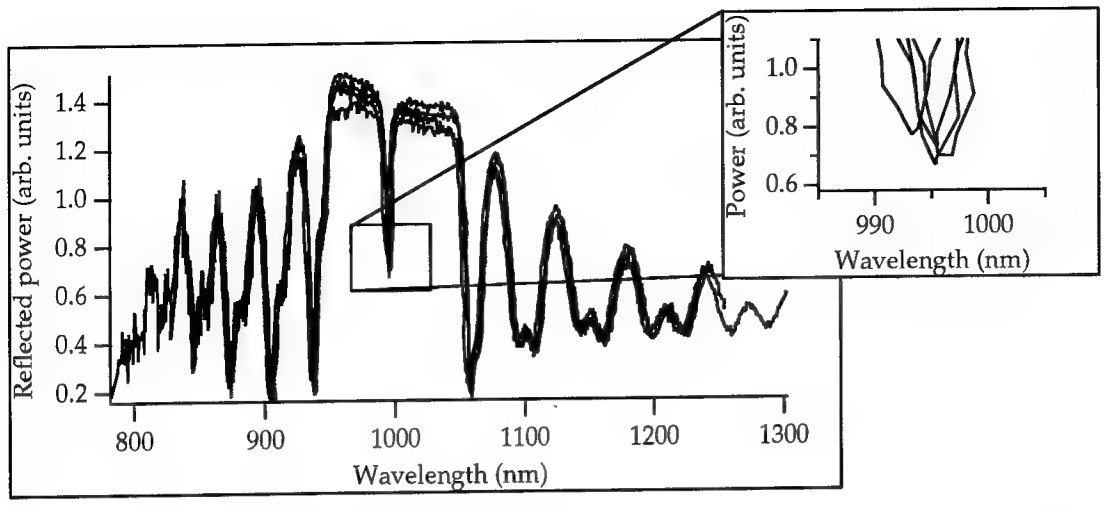

Figure 2.4: Reflection spectrum of a VCSEL at 4 places on the wafer

The use of an in-line calibration instead of an in-situ calibration has its advantages and disadvantages. The most important advantage is that it is a direct measurement of the final wafer at room temperature. In-situ calibrations rely on knowledge of mole fraction and refractive index data at standard growth temperatures (500-700°C). Although experience can relate room temperature results to these high temperature measurements, a large knowledge base is necessary before the system is ready for stand-alone use. A disadvantage for the in-line techniques is that it is much slower than the in-situ techniques after the appropriate knowledge base is established. The scope of this project and the lack of any prior experience with in-situ optical monitoring techniques favored the in-line technique as a first step. This system was shown to accurately measure, model, and predict working VCSEL structures using an appropriate calibration wafer. The ideal situation would be a combination of the two techniques that would evolve into the stand-alone in-situ calibration.

3. VCSEL FABRICATION

There are many different ways to fabricate VCSELs from the epitaxially grown material and thus many things to consider before starting. To be compatible with the rest of this project, the processing plan has to be compatible with bottom-surface emitting devices grown on SI wafers. The devices will be modulated up to approximately 10 GHz, must be contacted with Cascade probes, as well as be compatible with flip-chip bonding. Bottom surface emitting devices are necessary because the devices will be inverted before packaging and will thus have to emit upwards. These requirements practically eliminate a standard industrial process that uses ion implantation to isolate the devices[31]. Unless this implantation process is carefully designed, the electrical parasitics can limit the high speed performance of the devices. Also, the contact to the n-type material would require a wet chemical etch, alloy, or conducting implant after the isolation implant. This research, and most other research on VCSELs, uses mesa-style fabrication. The choice of either wet chemically etched or plasma etched devices depends to a large extent on how the devices will be electrically contacted.

For flip chip bonding onto a planar heat sink, the p- and n-type contacts on the device also need to be coplanar. For industrial applications where the thickness of the solder is 2 to 4 mils (1 mil = 0.001" = 25.4 μm), coplanar actually means coplanarity on the order of 1/2 mil is required, but, because of the thin solders (1-2 μm) used in this project, exact coplanarity was required. This requirement meant that the n-type contacts also needed to be on mesas. This contact design also made the devices compatible with CPW probes.

The most straightforward way to make the p-type contact to the heat sink was to put the p-type metallization on top of the VCSEL device mesas and bond them directly to the heat sink. This metal layer on the top of the VCSEL also increased the reflectivity of the top mirror stack[32]. Making contact to the n-type material is not as straightforward. The p-type material must be etched away so that an alloyed ohmic contact to the n-type mirror material can be made[33]. The etch needs to go past the quantum wells to the n-type material, but should be relatively shallow into the n-type material so that the electrons will not have to flow through very many Bragg layers, and also to reduce the thermal resistance of the structure. The required etch depth to contact the third $Al_{.1}Ga_{.9}As$ layer below the quantum wells (for the 1010 nm design) is 4.1 μm. With dry-etched mesas, that vertical step is almost impossible to cover (without using ~4 μm of

metal), but the sloped sidewall of a wet-chemically etched mesa (near 55° for H_3PO_4:H_2O_2:H_2O (3:1:20)) is easy to cover with metal.

There are disadvantages to these sloped sidewalls though. The current density is reduced at the active region of the devices due to current spreading. For large devices, the percentage change is small, but for a device with a 10 μm diameter top contact, the ~18 μm base results in the loss of at least a factor of two in current density. The undercut associated with a 4.1 μm deep etch also limits the smallest feature size to about 8 μm. Smaller devices were fabricated, but non-uniform undercut of the photoresist mask pinched off the tops of the VCSELs. Round and square devices with diameters (sides) from 8 μm to 60 μm were fabricated. Other round devices which lased through both a ring top contact as well as through the substrate were also made on the same wafer. Some of these top and bottom emitting devices have been sent to other research labs where independent research is underway[34,35].

All of the patterning of the VCSELs was performed using standard projection photolithographic techniques. The MANN GCA 6300 5:1 reduction stepper in the National Nanofabrication Facility (NNF) at Cornell University was used for all the steps in each process run. This project does not require fine feature sizes, and the large topography with the requirement of simultaneous exposures on the top of the mesas and the etched floor made the 5:1 reduction stepper the appropriate lithographic tool because it has a larger depth of focus (±2.42 μm at a feature size of 1.2 μm) than the 10:1 reduction machine. The four steps in the fabrication of the VCSELs are (1) zero-level alignment, (2) wet chemical etch, (3) n-type metallization and alloying, and (4) p-type metallization. The completed wafers were then thinned, polished, and cleaved into arrays.

Fabrication sequence

The epitaxial wafers were indium bonded during growth, so the first step in the fabrication was to remove the indium. The wafers were waxed, face down, onto glass disks and then put into warm HCl for 10-15 minutes. This removed the indium and left the back surface uniformly rough. Locally, the roughness is not constant, but over a large enough sampling region (the size of the die that would be used for processing), the wafer surfaces were parallel. No further back surface preparation was done before processing began. The 5:1 GCA stepper in the NNF is back-surface referenced and because almost every die processed was planar enough to have the 2 μm alignment marks develop correctly (these marks were the smallest features used on the

mask), the planarity was sufficient. The wafers were removed from the glass disks, cleaned, and reflectometry measurements taken. Then, 11-1/2 × 11-1/2 mm^2 square pieces were cleaved out of the regions of the wafer which were expected to lase. A solvent clean of a 5 - 10 minute soak in acetone and then rinses in acetone and isopropyl were performed before each fabrication step. Figure 3.1 shows a schematic of the process steps used.

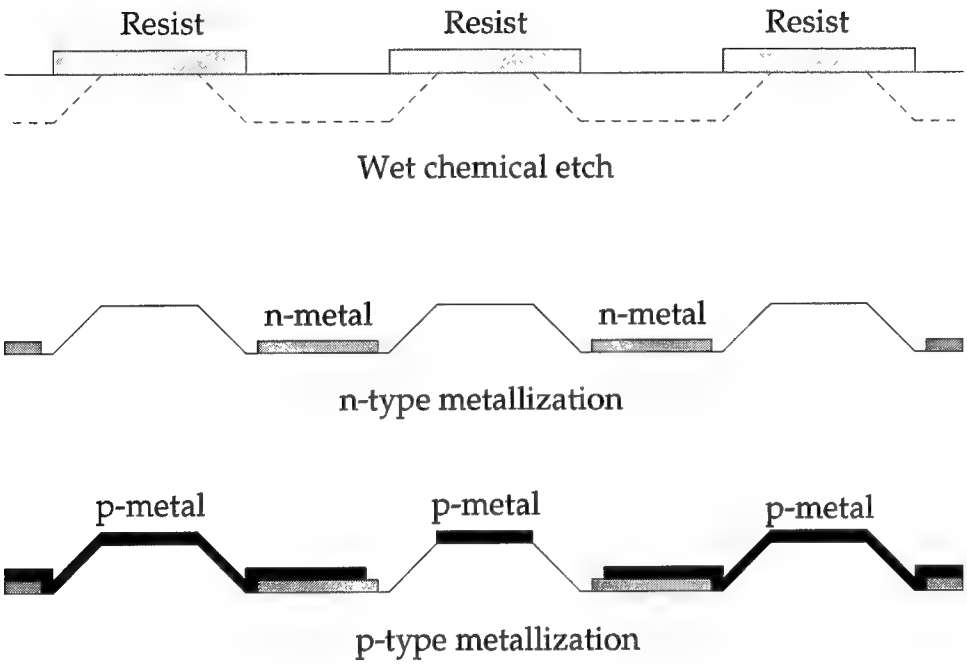

Figure 3.1: VCSEL fabrication steps

Zero-level alignment marks

Shipley C-20 Primer		4000 rpm	40 s
AZ5214-E	(~1.1μm)	4000 rpm	40 s
Hot plate bake 90° C		2 min	
Expose		0.93 seconds	
Hot plate bake 115° C		3 min	(reversal bake)
Flood exposure		60 s	
Develop in MF 321		~2 min	
Deposit		300Å Cr	

This photoresist needs only a hot plate bake and flood exposure to become a negative resist with undercut and thus capable of supporting liftoff. This makes the first step very fast. It can be completed in less than half a day. Feature sizes are very sensitive to the exact resist thickness and the time and temperature of the reversal bake, but for the alignment marks, the position is important, not the actual size (± a few tenths of a micron). Unfortunately, this is one of the photoresists that is slated for removal from the NNF supply. Similar results can be obtained through a standard image reversal process by using Shipley 1813 resist. Chrome metallization was chosen because it is inexpensive, easy to evaporate, and it sticks well to GaAs. It alloys with the GaAs during the alloy step, but it still has enough contrast to be used for alignment of the last level. The thickness of metal is not important as long as it is clearly visible.

Mesa definition

Dip wafer in NH_4OH:DI :: 1:15		10-15 s
Blow dry without a DI water rinse		
Shipley C-20 Primer	4000 rpm	40 s
Shipley 812 (~1.2 μm)	4000 rpm	40 s
Hot plate bake	115° C	1 min
Expose	0.37 s	
Develop in MF 321	~2 min	
Etch in H_3PO_4:H_2O_2:H_2O (3:1:20)	(1800-2000 Å/min)	

There was an interesting phenomenon that occurred while wet chemically etching the VCSEL mesas. As the layers of the Bragg stack were etched, its reflection spectrum changed and the perceived color of the stack cycled from the standard GaAs gray color, to purple, to a brownish yellow, and then back to GaAs gray. This effect was noticed only as the first few periods were etched away. During this period of color changes and continuing through the rest of the etch, it was observed that the high Al mole fraction materials had a much rougher surface than did the ones with low Al mole fraction. By counting these dark layers go by, a very accurate etch depth and stopping point could be achieved. The active region is a relatively long (1 wavelength instead of 1/4 wavelength) layer of GaAs and was used as a pre-endpoint endpoint indicator.

The etch was stopped on the $Al_{.1}Ga_{.9}As$ so that a better ohmic contact was formed. For the last process run, the etch was prepared somewhat stronger (3:1:12.5) and the endpoint of the etch was determined using only this visual technique. A surface profiler was used to document the etch depths only after the etching was done. This technique requires the user to be very alert for the endpoint, but was found to be faster and easier than the standard etching technique that uses regular surface profiling to determine etch depths.

An interesting, and unexplained, phenomenon was observed while etching these wafers. Parts of the wafer would etch much more slowly than others. This was easily observed because lines formed on the surface of the wafers, indicating an exposed layer of the rough $Al_{.9}Ga_{.1}As$, effectively made a contour map of the wafer surface. This etching phenomenon cannot be explained by differences in epitaxial layer thickness (which would only be a fraction of a percent across the ~1 cm die) or surface oxides (because the wafer starts etching uniformly and the effect accelerates during the etch). By holding only part of the wafer in the etching solution, the high parts of the wafer could be selectively etched away to correct the etch depth nonuniformity.

n-type metallization

Shipley C-20 Primer		4000 rpm	40 s
Shipley 1400-37	(~2.7 μm)	4000 rpm	40 s
Hot plate bake		90° C	2 min
Expose		0.45 s	
YES Oven image reversal			
Flood exposure		60 s	
Develop in MF 321		~2-1/2 minutes	
Descum in Branson (or Applied Materials [30 mT 30 sccm 90 W 10 s])			

Dip wafer in NH_4OH:DI :: 1:15	10-15 s
Blow dry without a DI water rinse	

Evaporate:

Nickel	100 Å
Au/Ge	900 Å
Silver	1000 Å
Gold	1000 - 2000Å

Standard image reversal techniques were used to form resist profiles with an undercut profile. The time between the oxide removal etch and loading into the evaporator was minimized to promote intimate metal/ semiconductor contact during the evaporation. This gold did not have to be very thick because it was covered with the p-type gold later in the process.

n-type contact annealing

In the RTA in Phillips Hall, Room 417: Anneal in $Ar:H_2$ :: 92:8
450° C for 10 s

The n-metal roughened after the anneal, but that is normal for this metallization. This step must be done before the p-metallization is put down or the p-metal will alloy with the GaAs and the roughened interface will adversely affect the mirror reflectivity.

p-type metallization

Shipley C-20 Primer 4000 rpm 40 s
Shipley 1650 (~5.5 μm) 3000 rpm 80 s (ramp the speed up slowly over about 20 seconds and spin at 3000 rpm for the remaining 1 minute)
Oven bake 90° C 30 min
Expose 0.7 s
YES Oven image reversal
HTG flood exposure 60 s
Develop in MF 321 ~2-1/2 minutes
Descum in Branson (or Applied materials [30 mT 30 sccm 90 W 10s])

Dip wafer in NH_4OH:DI :: 1:15 10-15 s
Blow dry without a DI water rinse

Evaporate:	Titanium	250 Å
	Platinum	200 Å
	Gold	2000Å
	Silver	5000 Å
	Gold	4000Å

As with the n-type metal, standard image reversal techniques were used and the time between the oxide removal etch and loading into the evaporator was minimized. The silver layer is included as additional solderable metal for the indium bonding process. Silver has better electrical properties and a higher thermal conductivity than gold so it is in no way degrading the thermal or electrical aspects of the contact and the 5000 Å is an inexpensive addition to the contact. A picture of a completed VCSEL mesa and its ground contact mesas is shown in Figure 3.2.

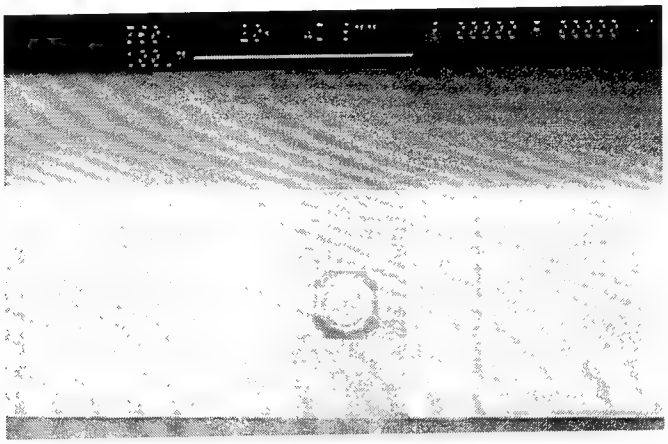

Figure 3.2: Completed VCSEL mesa with ground mesas

Back side processing

The completed wafers then needed to undergo back-surface processing which consisted of mechanical lapping and chemical polishing. Because the heat was to be extracted through the top contact of the device when flip chip bonded, and the smallest die to be cleaved is 450 μm wide, there was no need to thin the wafer very much. There will be some divergence of the laser beam in the substrate though, and a substrate thickness near 12 mils was used. The light will be coming through the back of the wafer so the surface also needs to be polished as smooth as possible to reduce scattering. If the mechanical lapping of the wafer is done carefully, there will be minimal chemical polishing to do. For the first VCSELs, a solution of Clorox® and DI water (1:10) was used to polish the wafers and satisfactory results were obtained. For the last run, a 1:500 solution of bromine in methanol was used. The Br:Methanol solution was much faster and easier, and produced similar results to the Clorox® polish. The Br:Methanol polish left the sample pincushioned, but because the wafer was still ~300 μm thick, this does not affect the devices.

Wet/dry process

The ideal VCSEL fabrication process should be compatible with all of the goals of the project and also use dry etching for the VCSEL mesas. There is a possible problem of ion-induced damage of the sidewalls from the dry etching, but chemically assisted ion beam etching (CAIBE) has been used by our group for fabricating very short (50-100 μm) etched-facet edge-emitting lasers for several years with much success. By using both wet and dry etching, the VCSEL mesas can be dry etched while the ground (n-type) mesas can be wet etched. The steps used in this procedure were only developed at the end of this project and were never implemented on real VCSEL material, but the process development and an interesting etch phenomenon will be presented here in order to give it formal documentation.

There is only one extra step involved in the change to a wet/dry process, the CAIBE etch of the device pillar, but three masks must be redone. The pads for the VCSEL p-type mesas were modified to be the exact size desired instead of including the necessary overhang required by wet etching. The mesa etch mask was tuned to the required etch depth, as will be discussed later in this section. And the p-metal mask was matched to the new VCSEL mesa sizes. A schematic of the process is shown in Figure 3.3. The notching after the wet etch will be explained in the next few sections.

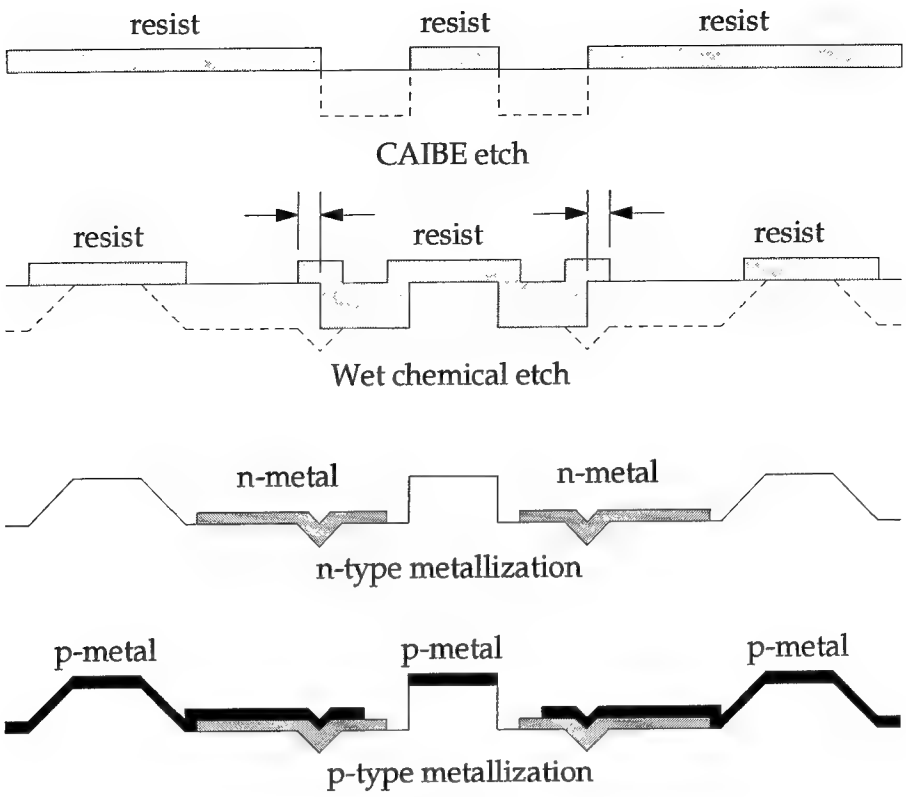

Figure 3.3: Wet/dry process

CAIBE etch

CAIBE parameters:	Cl_2	20 ml/min	
	Ar	2.5 ml/min	
	Current density	.2 ma/cm^2	(66 mA)
	Acceleration	500 V	
	Substrate temp.	110° C	
	Flow LN_2 through the shrouds during the run		

This is the process that has been used[36] ever since the load locking assembly was added to the CAIBE. The etch rate that was observed during these runs was 1350 Å/min, but these parameters usually produce a higher etch rate. The chamber pressure was unusually low during these runs and the lower Cl_2 pressure would be expected to produce a reduced etch rate.

The resists used for this process (AZ 4110 and AZ 5214) both gave vertical resist profiles, but both flowed during the 20 minute etch at 110° C. This flow affected the sidewall angle, but these were just dummy wafers and the process was continued.

Wet chemical etch

This step used the same resist process as described in Section 0 above, but it was necessary to tune the overlap of the CAD pattern in order to merge the wet and dry etches. A schematic drawing of the effects of different amounts of photoresist overlap is shown in Figure 3.4.

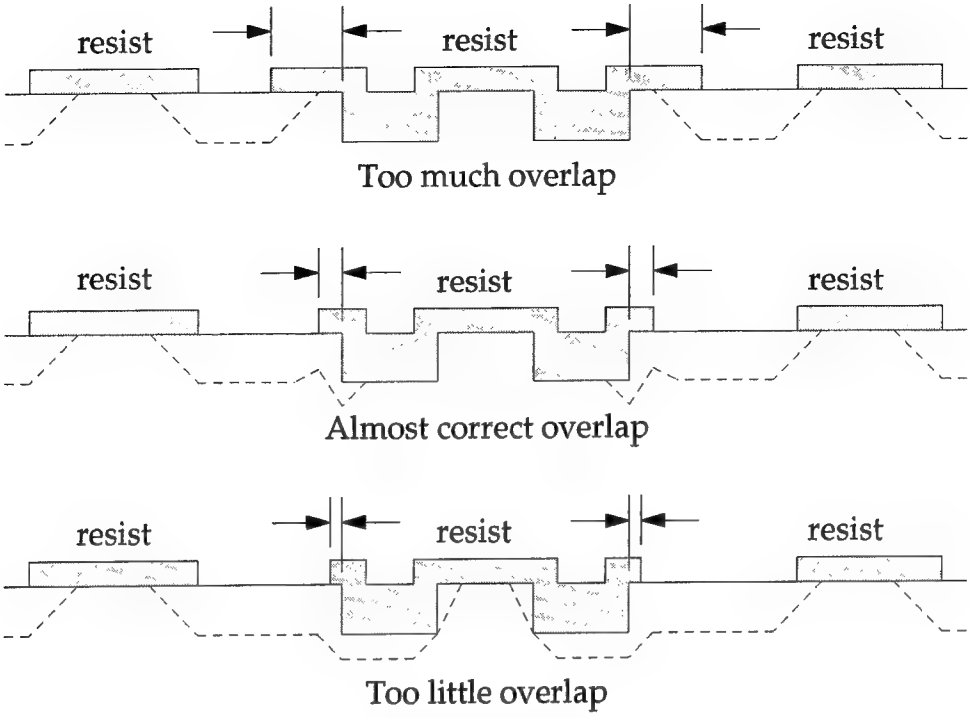

Figure 3.4: Tuning the overlap in the mesa etch

Too much overlap left fences around the devices. These fences have CAIBE inner walls and thus cannot be correctly metallized. An interesting etch effect was observed with all of the wet etches on wafers with correct or too little overlap. There was a crystal-orientation-dependent accelerated etch rate on the top and back side of the fence which formed a trench on the inside of the fence. SEM micrographs are shown in Figure 3.5 and Figure 3.6. The etch depths for the wet etch (left hand side of Figure 3.5 and right hand side of Figure 3.6) and dry etch are very similar (near 4 μm), but the trench was much deeper and the sidewall angles were different on the two faces. The depth of this trench can actually be a problem. If it was too deep, then it would electrically separate the n-type material that was being used for the laser ground contact.

The correct amount of overlap allowed the fence to be etched away in the same amount of time that it took to etch down to the n-type mirror. If the overlap was too small, then the accelerated etch rates on the inside edge of the fence rapidly undercut the resist and etched the VCSEL post. Although the 3:1:20 etch is relatively uniform, slight nonuniformities can easily affect the final etch profile as shown in Figure 3.5 which shows a non-uniformly etched fence in the center of

this figure and the remains of a VCSEL mesa on the left side. This can be avoided with proper overlap as shown in Figure 3.6.

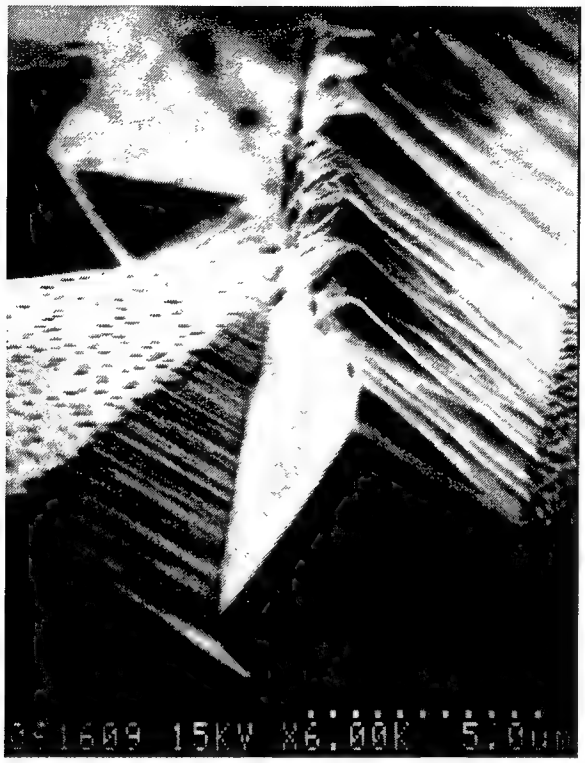

Figure 3.5: Nonuniform etching

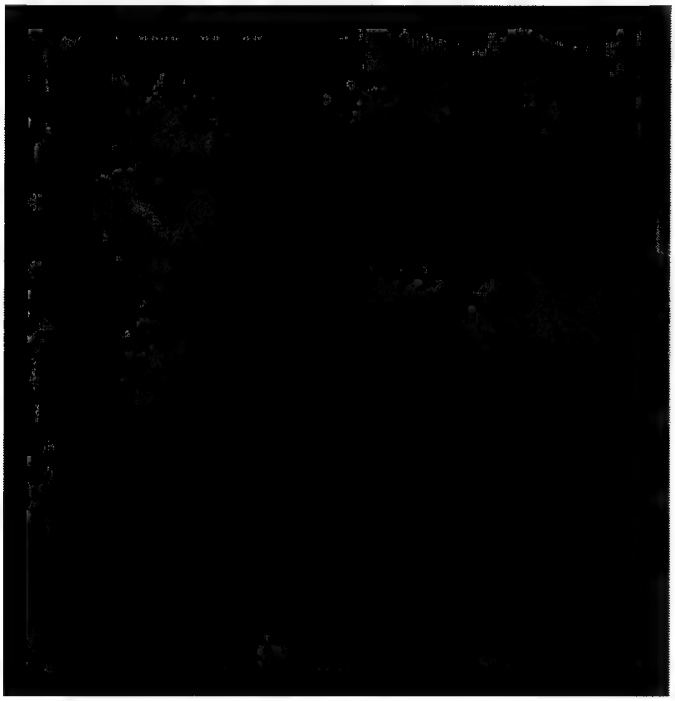

Figure 3.6: The result of correct overlap

For the devices shown in Figure 3.5 and Figure 3.6, the trench was much too close to the device. In order to ensure uniform current flow, there must be several microns of electrical contact between the n-type metal and the n+ $Al_{.1}Ga_{.9}As$ near the laser pillar. For the real VCSELs, n-type electrical contact was made on all sides of the devices, as shown in Figure 3.2.

The metallization and annealing steps proceeded as before, except for the additional challenge of putting metal on top of the VCSEL pillar. All SEM pictures of structures like Figure 3.6 showed good metal coverage while breaks in the metallization were common when any part of a fence remained.

The process used for these VCSELs was a simple three-step wet-chemically etched mesa style fabrication. It was appealing because of its ease of use, but it has strong drawbacks. Current spreading at the junction and light loss from the edges of the mesas will degrade device performance. These problems were addressed with the design of a new wet/dry process that uses dry etching for the VCSEL mesas and then uses wet chemical etching for the ground mesas so that a single thin metallization layer can be used to contact from the top of these mesas to the etched floor. Although not fabricated on real material, the process looks very promising and is compatible with the fabrication of dry-etched and cleaved edge-emitting lasers as well as with on-wafer high-speed probing and flip chip bonding.

4. HEAT SINKS

Properties and preparation of diamond substrates

Diamond wafers are the ideal choice for thermally conducting, electrically insulating, microwave substrates. Natural diamond (type IIa) is the best thermal conductor available with a thermal conductivity (σ_{th}) of 20-22 W/cmK[37] to go along with an electrical resistivity (ρ_Ω) of $>10^{12}$ Ω-cm. Natural diamond has the disadvantage of being relatively small and prohibitively expensive. Fortunately, thin films of polycrystalline diamond can be grown with high thermal conductivities and electrical resistivities by chemical vapor deposition (CVD; CVDD will be used as the abbreviation for CVD diamond). Depending upon the process, the supplier, and one's budget, CVDD can have a σ_{th} of 10-20 W/cmK and a ρ_Ω of $>10^{10}$ Ω-cm. Both types of diamond have a dielectric constant of about 5.6 which allows for realistic tolerances on lithography when fabricating waveguides for microwave frequencies.

Unfortunately, there are some drawbacks to using diamond as a heat sink for GaAs. It has a coefficient of thermal expansion that is 1/3 that of GaAs (2.3 vs. 6.5 ppm/°C), which makes bonding large die difficult. Small die, such as a small array of laser diodes or a few-transistor amplifier, is a way around this problem. Another drawback is the cost. With the recent large growth of the CVDD industry, prices have begun to fall, but a 1 cm × 1 cm piece of polished, metallized diamond substrate still costs between $250 and $800 (depending upon supplier, metallization, and σ_{th}). A 1 cm × 1 cm piece of diamond substrate is not realistic for small die but is suitable for batch processing of sinks.

There are several suppliers of CVD and natural diamond substrates, each with their own standards for thickness, size, polish quality, and metallizations. The material used in this project is from two different suppliers, Norton Diamond Film[37] (NDF), and GE Superabrasives[38] (GES). Both companies use different metallization techniques and with proper planning, both techniques were used effectively for fabricating heat sinks.

The metallization of diamond is a difficult process. Evaporated metals that normally stick to almost anything (Ti, Ti/W, Ni), usually do not stick to diamond at all. It is too chemically inert. NDF, however, has a proprietary process of sample preparation and evaporation conditions that promotes metal adhesion without any chemical interactions between the metal and the diamond. GES, on the other hand, uses a proprietary sputter process which guarantees adhesion through the formation of very strong diamond/carbide/metal bonds. The few hundred volt acceleration of a sputter deposition system tends to form metallic carbides at the diamond surface. These layers allow the metallization to adhere well to the diamond and are appropriate if a device will be bonded to the as-supplied sink. But, when the metallization is to be etched off to form isolated bonding pads, the metallic carbides remain, and the residual surface conductivity shorts the bonding pads together.

The material purchased from NDF was supplied with a Ti/Au (1000 Å/1000 Å) metallization on the top surface, and some pieces were metallized in house with an additional 5000Å of gold on the top and sides. This metallization was chosen because both Ti and Au can be easily wet chemically etched. The Pt diffusion barrier layer typically inserted between the Ti and the Au can only be removed in aqua regia or similar etchants, none of which are compatible with photoresist masks. Thus it was omitted for these wafers. The GES material was supplied without metallization for reasons which will be described in Section 0. All of the CVDD used in this project had a σ_{th} between 9 and 11 W/cmK.

Overcoming photoresist edge beads

The patterning of the CVDD used in this project was a technological challenge. Because of the relatively high price of CVDD (~$27 per 1.5 x 1.5 mm^2 die), only small sizes were financially feasible. 1.5×1.5 mm^2, 2.5×2.5 mm^2, and 1.5×5 mm^2 pieces from NDF were used in the following procedures. The small die required the development of a set of procedures that allowed patterning of the metallization on small substrates.

Spinning photoresist onto wafers generally yields a very uniform film over large areas. However, due to the viscosity of photoresist, a bead on the order of .5 mm to 1 mm thick forms at the edge of a wafer. This effect is typically of no consequence because processing is usually

done in the middle of a large wafer, but for the heat sinks used in this project, the edge bead covers the whole wafer.

Three techniques, encapsulation, tiling, and puddling, were used to make the small pieces of CVDD look like larger wafers. This moved the edge bead to the periphery of the assembly and a uniform film was formed in the middle where the diamond was located. The three techniques will be briefly described in the next few sections. There is a lot of promise for these techniques, but batch processing on a large CVDD wafer and cutting it up was by far the most time and money efficient technique.

Encapsulation

The encapsulation process involved mounting a heat sink in a layer of glue with the goal of keeping the top surface of the assembly flat and parallel to the top surface of the heat sink. This process, shown in Figure 4.1, gives a large, flat surface on which to spin photoresist. Squares of silicon wafers from 1/2" to 1" on a side were used as carriers, while the material that best served as the mounting tape was a material called Wafer Grip®[39]. Many different types of tape, ranging from common household cellophane tape to industrial Kapton® tapes, were tried with limited success. Wafer Grip® consists of a stable plastic backing with a thin layer of wax on one side. The stiff backing plastic of the Wafer Grip® kept the final surface of the encapsulation more planar than any of the tape schemes did.

The Wafer Grip® was placed on a hot-plate, wax side up, and heated to approximately 90°C, at which point the wax melted. The chip was then placed face down into the soft wax layer, and both were removed from the hot plate and allowed to cool. A few drops of superglue[40] were placed on top of each diamond chip, and a silicon square was placed on top of the glue. Many of the other glues tried were insoluble in all of the solvents used in standard semiconductor processing facilities. A small weight was used to keep the assembly flat and to squeeze out all but a thin layer of glue. The assembly was then allowed to cure overnight.

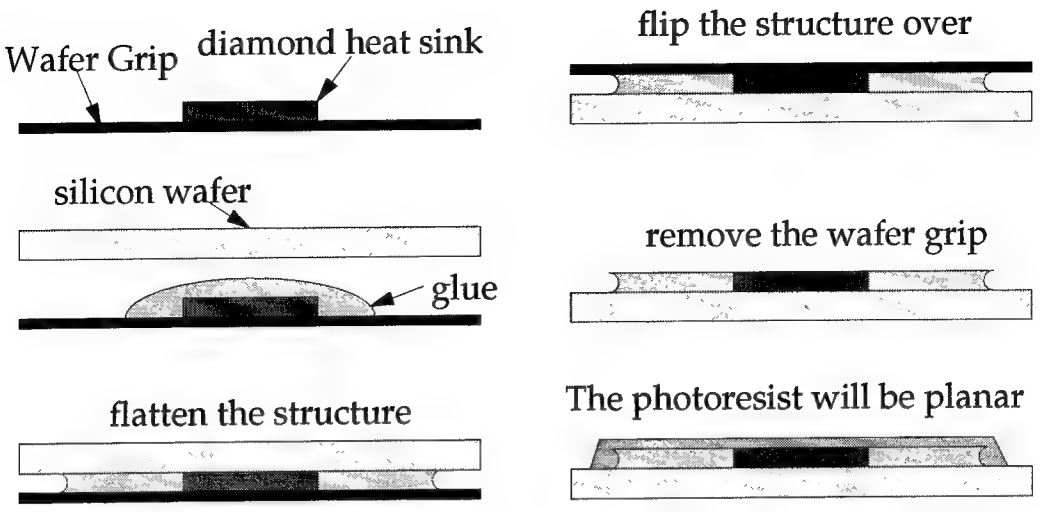

Figure 4.1: Encapsulation technique

After this drying stage, the assembly was re-heated on the hot plate to soften the wax, and the Wafer Grip® was pulled off. The encapsulation was then cleaned using a small amount of trichloroethylene or methylene chloride and a cotton swab. This did not completely clean the wafer (a thin film of the wax remained), so a standard oxygen plasma etch was used to prepare the wafer surface for later processing. After being patterned, the chips were easily removed from the glue encapsulation using acetone. Soaking for several hours or overnight is necessary at times, but all of the samples that were mounted in superglue were recovered after a few hours of soaking.

Tiling

The other mounting process, tiling, met with more success, but required some practice and a steady hand. This process consisted of using a standard photolithography spinner to dispense an adhesive compound onto a piece of silicon wafer. Then, the diamond chips were dropped into this layer and arranged so that they were all flush to each other with no gaps. The main challenge was to assemble the wafers without any glue getting onto their top surface and before the adhesive dried. Because of the large surface area, all of the interior wafers in the tiling were then edge-bead free. The edge wafers with the edge beads could be recovered and re-used for the next tiling.

The difficult part of this process is finding the proper type and thickness of gluing compound. The solvents in photoresists dry far too quickly to allow any time to mount the samples, and the solvents are typically carcinogenic. Most of the other glues tried were simply too thick to spin onto a wafer. The material that worked best was a thick polyimide formulation. (Spin Ciba-Geigy Probimide 287 at 3200 rpm for 30 seconds. After positioning the wafers, bake at 90°C for 30-45 minutes.) This material dried slowly enough to allow the assembly to be adjusted and allowed large (>15 pieces) tilings to be formed. Methylene chloride or n-methyl-2-pyrrolodinone was used to soak the diamonds out of the polyimide after processing. The heat sinks fabricated for the microwave tests and the initial flip chip bonding experiments were mounted using this tiling technique.

Puddling

The third process that was tried, puddling, is similar to the encapsulation scheme above. The diamond is dropped into a puddle of some type of glue (photoresist), which is then allowed to dry. The glue around the sample increases the effective area of the sample and will move the edge bead off the wafer. This is actually the simplest of the three techniques and, although it does not promise high yield, its ease of use makes it appealing. A puddle of photoresist is placed on a carrier (1/2" × 1/2" Si wafer). A resist was chosen with a suitable viscosity such that the combination of sample thickness, relative density of the diamond and the resist, and surface tension allowed the sample to sink to the bottom of the puddle, but still have a ring of resist around it as shown in Figure 4.2a. Other possible outcomes of this process are shown in Figure 4.2b, where too little, too much, and far too much resist have been used in the process. The assembly is then carefully put into a 90° C oven for 1/2 hour.

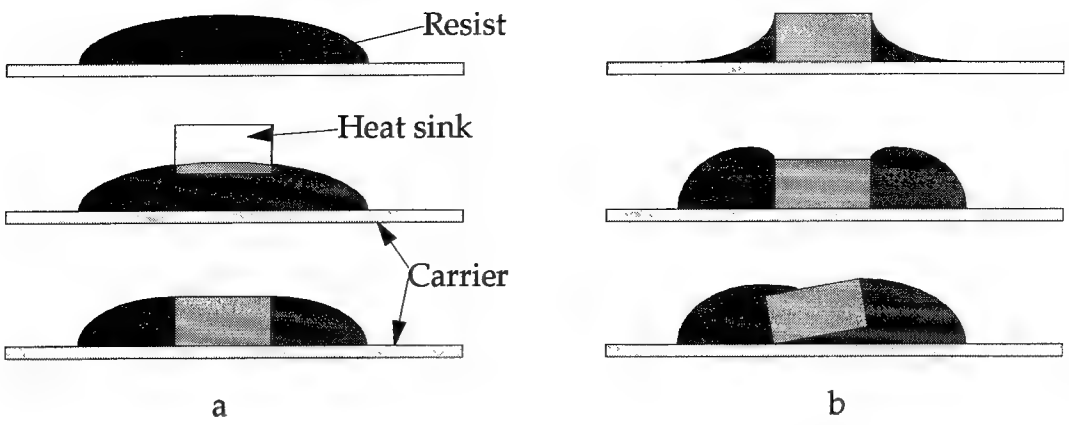

Figure 4.2: Puddling sequence

a: mounting a die using the puddling technique

b: possible outcomes when using too little or too much photoresist

A problem with this technique is that bubbles in the resist will expand when the samples are put under vacuum in the descum and evaporation steps. A possible solution is to eliminate the bubbles from the resist using a desiccator and mechanical pump. This method of removing bubbles works well for epoxies because they cure by chemical action instead of solvent evolution. But, for photoresist, the solvents are rapidly evolved from the surface of the resist, and a hard skin of resist forms over a puddle of wet resist. Unfortunately, no epoxies that were compatible with the viscosity and temperature requirements of the process could be dissolved at the end. Although the expansion of bubbles in the resist reduced the process yield, almost all of the small diamond heat sinks used for bonded device testing were fabricated using the puddling technique.

Heat sink pattern design

In order to make high speed connections to the flipped devices, a type of waveguide was needed. The obvious choice was coplanar waveguides[41,42] (CPWs) because CPWs are directly compatible with flip chip bonding and because of previous experience with low-parasitic probing of lasers and transistors with CPW microwave probes[43]. A coplanar waveguide is a style of microstrip line that consists of three conductive stripes, all on the top surface of a dielectric. The center conductor is surrounded by gaps of equal width, which are then surrounded by semi-infinite ground planes. A CPW structure is shown in Figure 4.3.

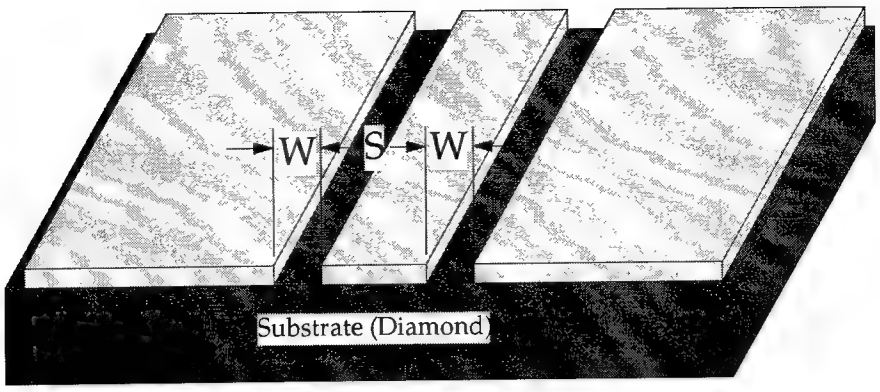

Figure 4.3: Coplanar Waveguide (CPW)

The fabricated wafer was flipped over and soldered onto the CPW. Then, a positive voltage was applied to the center conductor while the outer ground pads were electrically shorted and connected to the system ground.

The impedance of a CPW is a function of the ratio of the center conductor width to the ground plane separation, S/(S+2W)[42]. Using the dielectric constant of the substrate and a center conductor width that was compatible with our probing techniques (44 μm), gap dimensions (10 μm) were determined to give the desired 50 W transmission lines[42,44]. A convenient way to fabricate both the VCSELs and the diamond heat sinks was to make a linear array of devices on 200 μm centers. The spacing of 200 μm was chosen because Rome Laboratory has a supply of 100 μm pitch CPW probes. The resulting pattern was a series of these CPW structures where adjacent devices shared ground planes. This sharing of contacts was not a problem in practice because only one device was probed at a time. With the dimensions determined, photolithography was used to transfer the pattern into the metallization.

As mentioned previously, standard wet chemical etch formulas for Au and Ti were tried first because of their ease of use. The side-effect of all wet etching techniques, however, is undercut, a result of the exposure of the sidewall to the etchant after the etching has begun. In the ideal situation an approximately 45° angled sidewall profile would be expected.

One important factor that determines the resulting sidewall angle is the adhesion of the photoresist to the underlying film. If the adhesion is poor, there are localized areas where the etchant can penetrate farther under the resist, which quickly leads to severe undercut.

Unfortunately, the adhesion of the photoresist to the gold was typically poor and for a 6000 Å etch depth, an undercut of 4-6 μm was typical. A diamond heat sink after the gold etch and before the removal of the photoresist is shown in Figure 4.4.

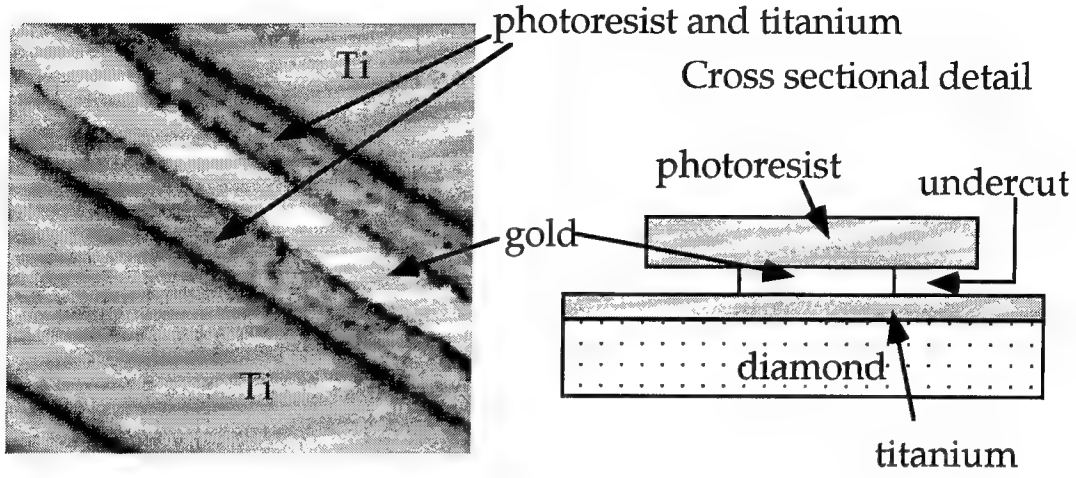

Figure 4.4: Extreme undercut after the wet etch

The titanium etch (2 ml HF in 100 ml DI H_2O) behaved as expected. After an initial delay of 8-10 seconds, in which the oxide layer is removed, the exposed titanium surface bubbles and is etches away. The wafer is then immediately removed from the HF:DI mixture and rinsed in DI water to minimize undercut.

A dry etch technique for gold was then investigated. There are no known reactive ion etching techniques for gold, but simple ion bombardment of the surface, sputtering, is an effective technique. More specifically, this technique is called ion milling and consists of an energetic stream of ions (typically argon) directed toward the sample. The ions are neutralized by a hot filament before impacting the sample to eliminate charging effects on insulating samples. The impinging atoms sputter both the photoresist and the gold, so knowledge of the relative sputter rates (gold ~1000 Å/min; photoresist ~250 Å/min) and desired etch depth is necessary to determine the thickness of photoresist necessary to protect the CPW lines during the etch. To ion mill the 6000 Å of gold so that no isolated traces were visible took 6-3/4 to 7-1/4 minutes (500 V, 1 mA/cm^2). The endpoint for this etch was easily monitored because of the different colors of gold and titanium.

The photoresist mask was removed in an oxygen plasma (~2000 Å/min at 500 V, 30 sccm O_2, 30 W/cm^2), and then the previously mentioned titanium etchant was used to isolate the lines. There is another important property of diamond that must be considered here. Diamond is not the lowest energy form of the carbon lattice, graphite is, and ion damage from an RIE system can polymerize the surface of the diamond into conducting graphite, thus shorting out the bond pads. Hence, it was important to strip the photoresist before removing the Ti so that the diamond was never exposed to an ion plasma.

The final step in the process was the evaporation of a suitable solder onto the ends of the CPWs. Indium was chosen as the solder material for this project and solder thicknesses between 1 and 2 μm were used. All indium evaporations used standard photolithography and liftoff. A completed heat sink for a 2×8 array of VCSELs is shown in Figure 4.5. A detailed explanation for the choice of indium solder, deposition techniques, and appropriate thicknesses is provided in the next section.

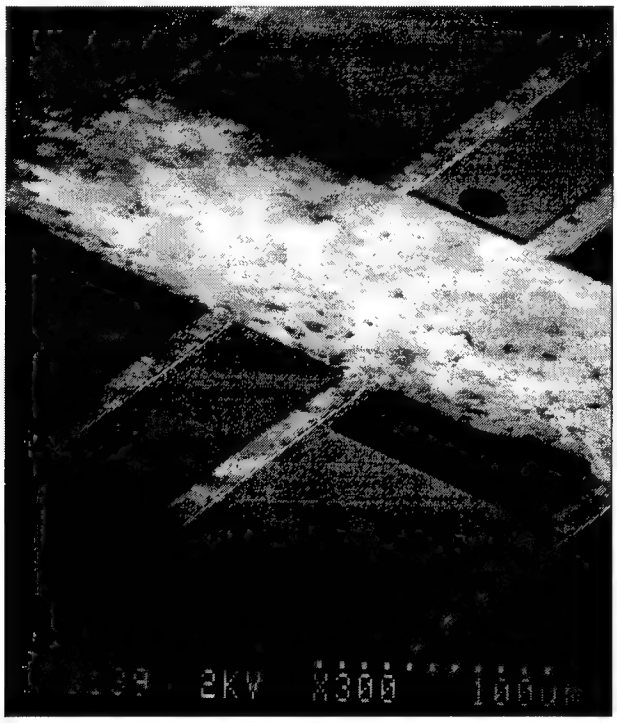

Figure 4.5: Heat sink for a linear array of VCSELs

Two-dimensional arrays of devices, as shown in Figure 4.6, were also fabricated from the same epitaxial material as the linear arrays, and these 4×4 arrays needed appropriate heat sinks as well. The odd ground configuration was designed to connect all of the VCSELs to a common ground while not interfering with the 16 coplanar waveguide center conductors on the heat sink. These arrays were fabricated using the design rules of the VOI project at Rome Laboratory which required emitters on 200 μm centers. The design of the CPWs for the outer 12 devices was the same as for the linear array heat sinks, but for the inner devices, the CPWs needed to be tapered to fit between the outer devices and their contact pads. The same S/(S+2W) ratio was maintained during the taper, and the taper length was made as long as possible, so an impedance near 50 Ω with no microwave reflections was expected. Figure 4.6 shows an SEM micrograph of a 4×4 array of VCSELs and Figure 4.7 shows its heat sink.

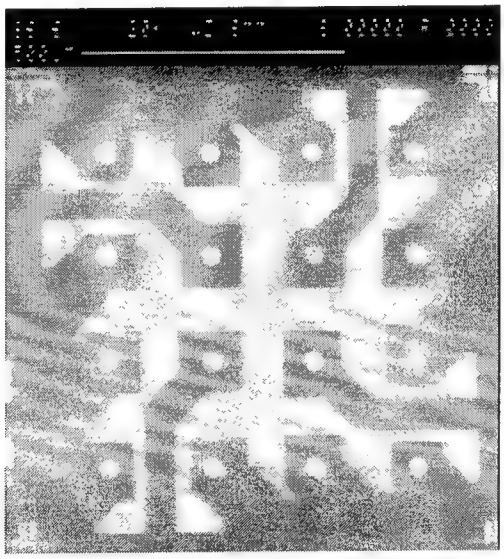

Figure 4.6: 4×4 VCSEL array for the Rome Laboratory VOI project

Figure 4.7: Diamond heat sink for 4×4 array

Batch processing on 1 cm^2 diamond

An obvious solution to dealing with the small parts mentioned above is to use bigger pieces of diamond and pattern many die on each piece. About halfway through this project, this idea became a reality. The two difficulties with this process are (1) being able to afford big pieces of diamond, and (2) the fact that diamond cannot be cleaved. The CVDD is polycrystalline and must be either sawn or laser-cut. Sawing is a slow, dirty process with typically a large kerf loss and not enough positioning accuracy to get the die close enough together to take advantage of the economy of scale afforded by 1 cm^2 diamond. A laser-cutting service was required. GES is very knowledgeable in the field of laser-cutting diamond both before and after processing. The difficulty in post-processing laser cutting is that the process of laser ablation of the diamond leaves behind a residue of conducting graphite. This layer is on all of the cut edges and is also deposited onto the top surface. An encapsulation layer is necessary to make sure that the CPW lines remain electrically isolated. Therefore, with a diamond cutting service available, a process for fabricating heat sinks on 1 cm^2 diamonds was developed.

The diamond from GES was supplied double-polished without any metallization. Their metallization process forms a strong metallic carbide layer on the surface of the diamond so liftoff instead of etching had to be used. They also have a proprietary process of resist development and sputter parameters that results in liftoff. In order to save the expense of having GES fabricate our sinks, several different photoresists with different thicknesses and edge profiles were prepared on silicon wafers and shipped to them. They tried a sample metal deposition and returned the samples. Liftoff was performed, and an acceptable process was determined. (Shipley 1813, 2000 RPM, ~2 μm thickness, bake 115°C 1 min, expose .4 sec, develop in MF321:DI::1:1 for 50 sec with slight agitation.) The CPW pattern was developed on a few diamond wafers and they were shipped to GES for a metallization of 1000 Å TiW / 5000 Å Au. These pieces were returned to us, and liftoff was performed. The results were not perfect, and some wafers had wings at the edges of the metallization, but all the pieces continued through the process. Standard photolithography was used for liftoff of 1 μm of indium solder. The wafers were then protected with a layer of photoresist and shipped back to GES for laser cutting. At GES, the wafers were glued to a glass slide, cut, and sent back without demounting the small dies. The individual dies were soaked off the glass slide in acetone which also removed most of the photoresist protection layer. Local heating of the resist along with the re-deposition of graphite near the edges of the die occurred as a result of the laser cutting. Thus, a lot of material remained after the acetone soak. Extended ultrasonic acetone cleans (30 min - 1 h) were necessary to clean the dies.

Electrical results

Measurements of the die produced by each of the above processes typically showed electrical isolation of > 10 MΩ, except for the GES wafers. Because of the less-than-perfect TiW/Au liftoff, the gold wings resulted in non-ideal solder-level lithography, and some indium shorts between pads were observed. There was also some residual conductivity after the acetone clean of the wafers that was probably due to residual graphite debris. The residual resistance, for the CPWs that were not shorted or open, was typically between 20 and 75 kΩ. This residual conductivity should not affect either DC or microwave measurements to a large degree because the resistance of the devices is near 350Ω.

Microwave characterization was performed on specially designed die. These die have long (~5 mm) CPWs in order to obtain a more accurate measure of the loss in dB/cm of this type of waveguide on diamond. It was found that diamond is an excellent microwave substrate with almost no loss. A loss of 0.24 dB/cm was measured at 30 GHz[45], and this loss can be totally attributed to resistive losses in the metal[44].

Although the initial experiments with small diamond chips resulted in many usable heat sinks, moving to a batch process fabricated more die (literally hundreds of die) in a much shorter time (only a few days of work over the course of a couple months of shipping material back and forth). The processing on the large pieces of diamond needs to be improved though. The attempt was to try to pack many die on each 1 cm^2 piece, but the packing might have been a little bit too high as evidenced by the residual conductivity of many of the lines. There were also edge-emitter heat sinks on the batch processed die and these suffered more than the VCSELs because of the requirement of mounting the edge-emitting laser very close to the edge of the sink. With a little less ambitious spacing of the die, VCSEL heat sinks should be easy to fabricate on diamond, and the wings resulting from imperfect liftoff of the sputtered Ti/Au will not affect yield to a large extent.

5. FLIP CHIP BONDING

Flip chip bonding is a method of attaching a die to a carrier in which the die is inverted and soldered, junction-side down, onto the carrier. This method of bonding is an excellent way both to eliminate one level of wire bonds and to obtain very good thermal contact between the junction and the carrier. If the carrier is a multi-layer high density alumina board or, even better, diamond, then the improvements in thermal conductivity can be immense.

IBM has capitalized on flip chip bonding since the late 1960's when they developed the C-4 process[46]. C-4 (controlled collapse chip connection) uses the surface tension of the solder alloy and specific land metallizations to pull the chip into very accurate alignment with the carrier. This process allows high-throughput, medium-accuracy tools to be used for chip placement while the fine alignment is accomplished in the reflow process.

The C-4 process uses thick solder (typically > 50 μm) and bond pads of at least $50 \times 50\ \mu m^2$. Without creating a solder damming layer on both the sink and the device, these thicknesses of solder are not possible with the high packing density of the RL VOI project. In order to remain compatible with the fine pitch design rules of the VOI project, much thinner layers of solder were used on the heat sink, and the contact areas on the die were limited to the size of the top of the active VCSEL regions. Figure 5.1 shows a schematic result of using 2 μm of solder for the 4 μm VCSEL mesas. The solder that is pressed out from the contact areas can alloy with the sides of the mesa and can affect electrical performance of the devices to the point of shorting them out if the indium contacts across the junction. Figure 5.2 shows an area of a heat sink where a device has created a deep depression in about 1 μm of In. The VCSELs used in this research are actually not circular, but octagonal (or 10- or 12-sided) as shown by the impression in the indium in Figure 5.2. This is due to mask-making considerations and the variations from circular VCSELs are considered insignificant. Thick solders were not used because it was found that nearly perfect yield could be achieved with just 2 μm of solder.

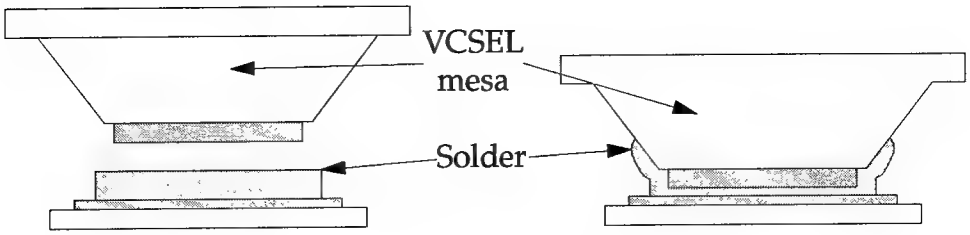

Figure 5.1: Thin solder for VCSEL bonding

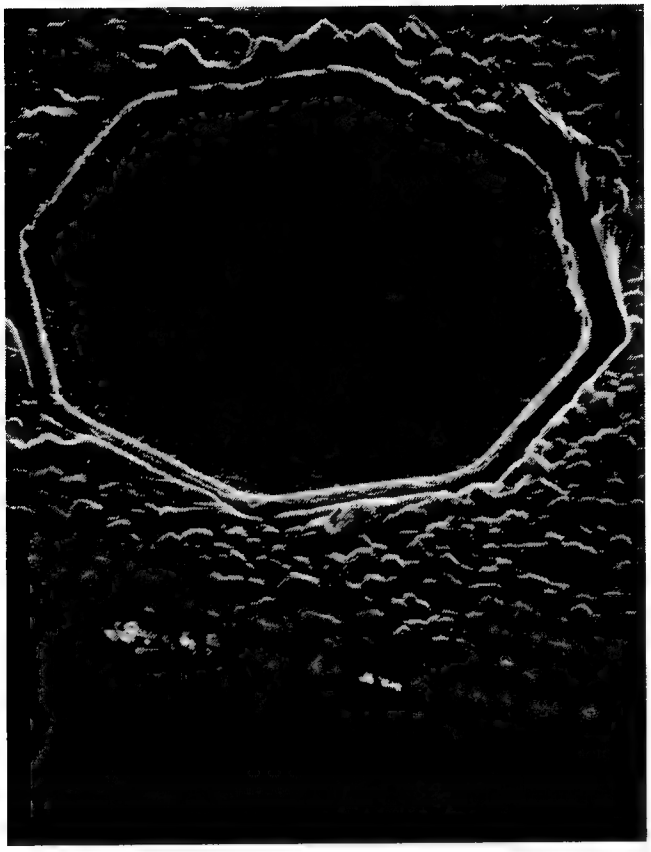

Figure 5.2: VCSEL depression in indium

The rest of this section describes the choice of solder and its deposition technique as well as the development of the bonding process, a description of the flip chip bonder, and the procedure used to bond the devices.

Solder

With the many choices of solder used in commercial bonding processes, narrowing the list down was the first priority. The C-4 process mentioned above typically uses Pb/Sn alloy solders, whether it be the eutectic (m.p. 183°C) or the higher melting point 95/5 alloy (m.p. 310°C). The properties of these materials are well characterized and because of the many high-volume consumers, the materials are very inexpensive. But, for our in-house deposition, the choice was made to avoid Pb-based solders for toxicity reasons.

Some of the non-Pb-containing alloys that are used in flip chip bonding applications include In (m.p. 157°C), In/Sn alloys (m.p. 115°C to over 300°C), and Au/Sn eutectic (80/20 m.p. 278°C). Indium was chosen as the flip chip solder for the ease of evaporating a single-component solder, the easy availability of high purity indium in an MBE lab, and the large expense of Au/Sn (~$800/oz) and In/Sn (~$500/oz). Indium is also known to readily form alloys with gold[47,48,49,50,51,52], the top metallization on both the heat sink and the VCSEL die. Because of the very small size of the die to be bonded (900 μm × 900 μm and 450 μm × ~1.8 mm), the fact that they will only be tested for limited periods of time, and the fact that they will not be undergoing thermal stress tests, the properties of fatigue strength[53] and long-term stability of the bonds were not important design issues. An ingot of Au/Sn was purchased to be used in the next generation of bonding experiments[54,55] in order to address the problems of oxidation during bonding, thermal conductivity, and long-term stability of the contact.

The first challenge to using any of the above solders is depositing the film so that it maintains all of its expected reflow properties. The problem is finding a lab manager who will let you deposit indium in the lab's evaporator. A common misconception is that indium has a high vapor pressure. In reality, as most MBE growers are well aware, In does not have a high vapor pressure, just a low melting point. But, indium oxide has both a very large surface area and is very hydrophilic. Thus an evaporator coated with indium (oxidized) tends to be very gassy, needs extended pumpdowns, and may never attain acceptable base pressures.

Because of the available deposition chambers, thermal evaporation was used to deposit indium. A thermal basket evaporator and an e-gun evaporator were available on campus. The thermal evaporator was dedicated to solder evaporations and was thus tried first. The system is a small bell jar pumped by a diffusion pump, backed by a mechanical pump. Due to infrequent use of the cold trap, high concentrations of oil vapors in the chamber were suspected. Also, there was

no shutter in the machine which resulted in poor quality material being deposited before the charge and basket had a chance to outgas. Films deposited in this machine did not reflow. The film from the e-gun evaporator were much better, but long pumpdown times, inconvenient access to the machine, and the almost total lack of control over the evaporation rate due to the high power e-gun forced another solution.

A used evaporator became available for use as an experimental solder evaporator. Its history was unknown and it had no tooling so it was disassembled, cleaned (including an aqua regia etch of the bell jar), and custom tooling was designed. The next section describes the evaporator and the evolution of a deposition technique that produced specular indium films.

Solder deposition

The evaporator that was used to deposit solder is a 3-hearth thermal evaporator, which was usually loaded with chrome, indium and gold. The pumping system, bell jar, and feedthroughs are a Veeco VE-401 manual evaporation system. The system is pumped by a mechanical pump and a 2200 l/s diffusion pump using Corning 705 diffusion pump oil, and has a LN_2 cold trap between the chamber and the diffusion pump. The cold trap was used for all evaporations and test pumpdowns of the system. All of the new tooling was made of 304 stainless steel and was thoroughly degreased before assembly. The base pressure of the chamber was 2×10^{-7} (below the original 5×10^{-7} original specification) and a pressure of 5×10^{-7} was routinely achieved after 2 hours of pumping. If, after attaining base pressure, the main gate valve was closed, there was a steady pressure rise in the chamber. By observing the leak-up rates as a function of pumpdown time, significant outgassing was observed as well as the possibility of a small leak, but the oxygen partial pressures were still considered very small and with proper evaporation technique, films with expected melting points were routinely produced.

The first evaporations were performed using techniques similar to standard contact metallizations, at deposition rates of a few (4-10) Å/sec. These evaporations always resulted in white, rough films. The white color was a result of both the surface roughness and the presence of InO. The roughness was sometimes thicker than the expected film thickness. The material also did not melt, rather it showed only small changes in surface structure with no flow occurring.

It was decided that the film was becoming too hot during the evaporation. For a certain thickness of deposited material, the total energy imparted to the sample is proportional to the sum of two terms

$$\text{Energy} \approx (\text{radiation\_heating} * \text{time}) + \{(\text{heat\_of\_sublimation} + \text{metal\_temperature}) * \text{thickness}\}.$$

Because vapor pressure rises exponentially with temperature, the first term could be greatly reduced while only slightly increasing the second term by evaporating at higher rates. Higher evaporation rates were tried with a constant film thickness and film quality improved. It was also observed, by comparing films deposited before and after a major leak was repaired, that the indium films were very susceptible to oxidation. Long pumpdowns and evaporation rates above 75 Å/s were used to produce the best films. Rates up to 150 Å/s were tried and results were marginally better as the rates were increased to this level. The higher evaporation rates also result in extreme outgassing of the alumina baskets. Thus, the baskets were filled to capacity and 1/2 to 1 μm of material was deposited onto the shutter as the basket was outgassed and an evaporation rate was established.

Results for thick (2 μm) and thin (~.1 μm) films were very similar, both in degree of specular reflection and by observation under an optical microscope. Evaporations on silicon wafers both with and without a native oxide produced similar results. A 1 μm thick film as viewed through an optical microscope (~1000×) is shown in Figure 5.3.

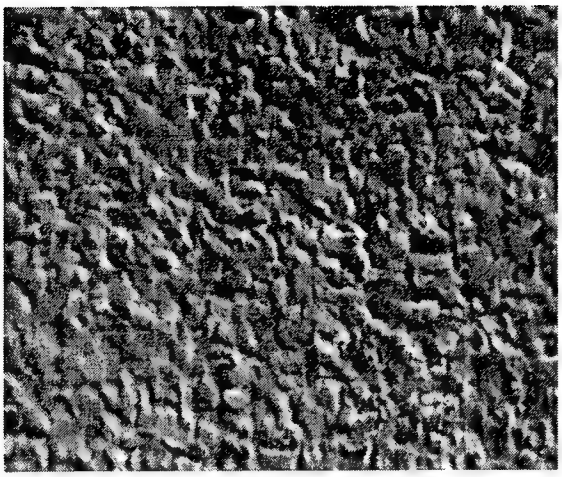

Figure 5.3: Indium on silicon (optical microscope)

Shadow masks were used to form dots of indium to evaluate the melting point of the films, and the dots of indium melted nicely at temperatures near the expected 157°C. With perfected films on silicon wafers, deposition onto gold had to be developed. The indium solder was to be deposited onto the diamond heat sinks, directly onto the gold metallization layer. Because the indium deposition temperature is above the formation temperature of almost all of the In/Au alloys on the phase diagram[56] , alloying during deposition was expected. The Au/In phase diagram is shown in Figure 5.4.

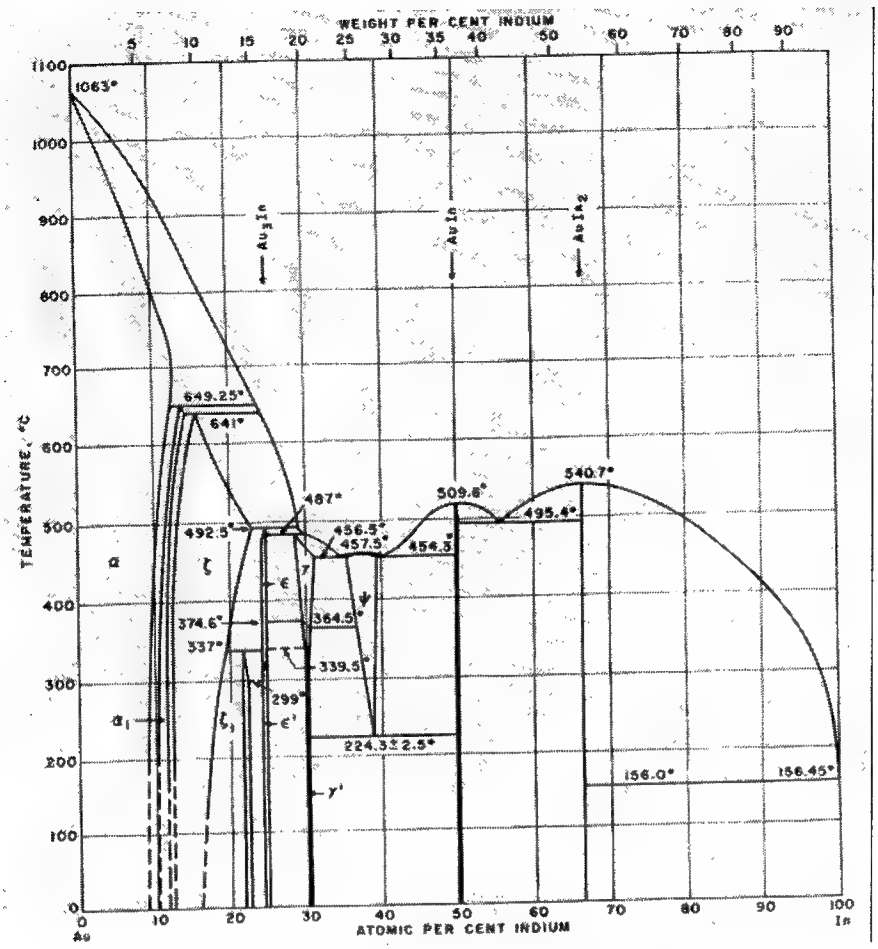

Figure 5.4: Gold/indium phase diagram

The In that was deposited on Au always looked white, but this was due to surface roughness of the crystalline AuIn alloys, as seen in Figure 5.5, and not due to oxidation. The indium was etched off the gold and the resulting surface showed similar, although much smaller crystalline structure, as shown in Figure 5.6. This alloying was always observed and was reduced only slightly by evaporating at 150 Å/s. This alloying effect is well known and was to be used to bond the indium to the gold on the VCSEL. An indium pad on a gold CPW after annealing is shown in Figure 5.7. The pre-alloying of Au and In as well as the continued alloying during the reflow cycle raised the melting point of the alloy far above that of pure indium, though.

Figure 5.5: Indium on a gold CPW

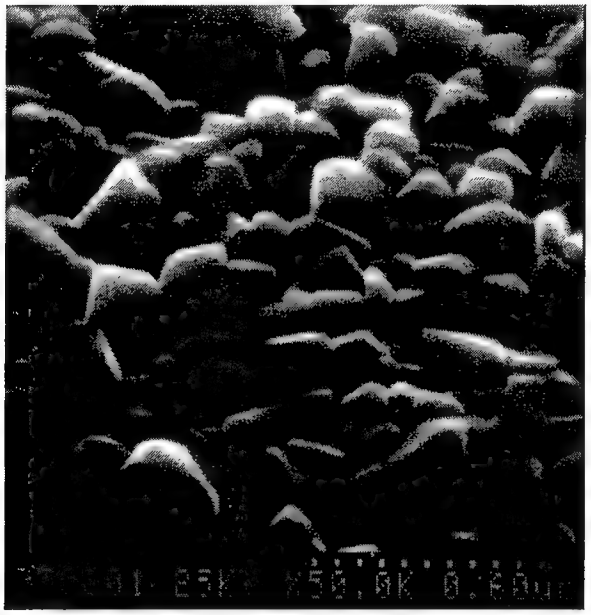

Figure 5.6: Indium/gold interface (etched)

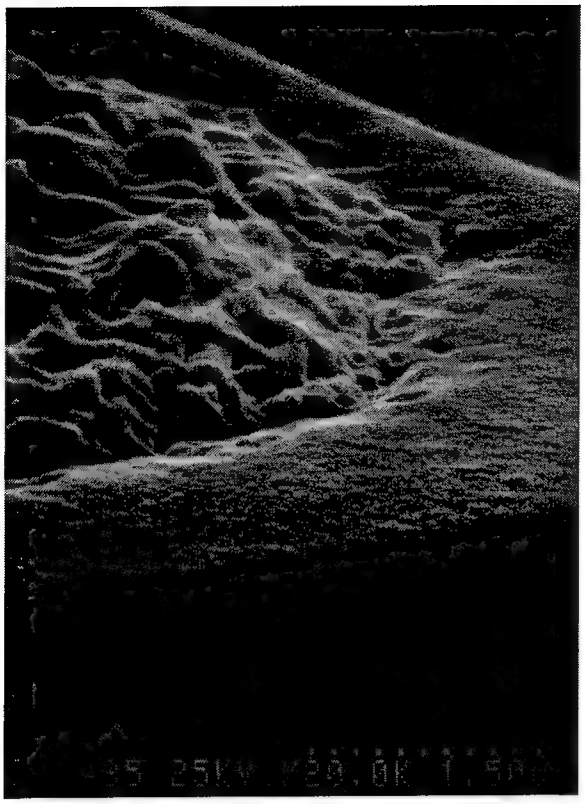

Figure 5.7: Alloyed In on Au

A simple diffusion barrier[57] that could be deposited in the same chamber as the indium was needed to address the problem of pre-alloying. Possibilities for a diffusion barrier included Ni, Cr, and Ti[58]. Chrome was chosen because it was already being used in the chamber as an adhesion layer for Au on Si evaporations. Chrome has a poor thermal conductivity (~1/4 s_{th} of Cu), but only thin layers ~500Å were to be used so it was not expected to adversely affect the heat sinking. Again, using a shadow mask, Cr/Au, In/Cr, In/Au, and In/Cr/Au layers were made.

By evaporating through the shadow mask at different angles, all of these combinations could be produced on the same wafer in close proximity, making relative comparisons easy. Cr/Au showed no metallurgical interaction after evaporation or after annealing. In on Cr was rougher than just In on Si wafers. Figure 5.8 shows an In/Cr film after annealing. While the changes caused by annealing the film 20-30° C above the indium melting point were minimal, the plate-like structures were present both before and after annealing and tended to form random tall peaks for unknown reasons. In/Cr/Au showed similar structures and peaks.

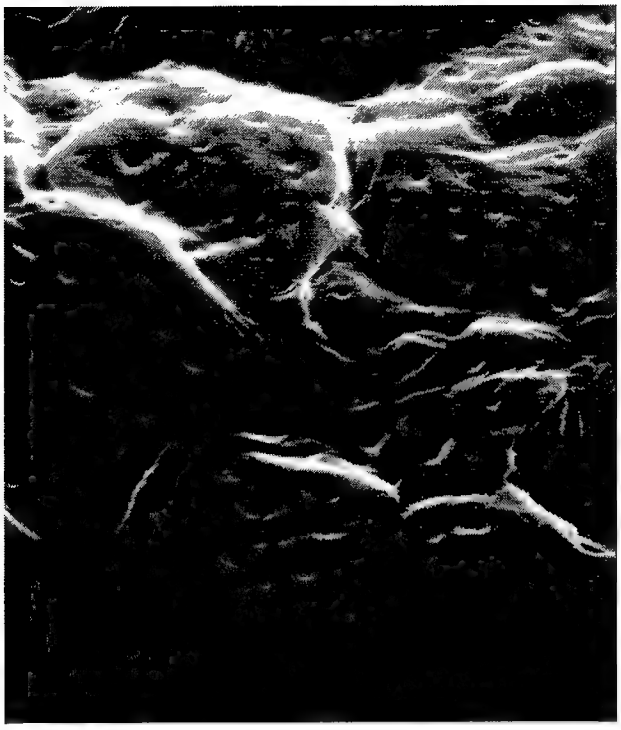

Figure 5.8: In/Cr after annealing

Upon annealing, the utility of the diffusion barrier became apparent. The In/Au alloying was significantly reduced as is shown in Figure 5.9 In/Au is on the left hand side and In/Cr/Au is on the right hand side of the figure. Although these results were promising, Cr diffusion barriers were not used for any of the real bonded devices because of the lead time involved with fabricating the GES diamond sinks. For all of the samples tested, the alloying effects without the diffusion barriers were sufficient at reflow temperatures within 100° C of the solder melting point to produce good bonds.

Figure 5.9: In/Au - In/Cr/Au lateral interface (top view)

Flip chip bonding

Initial tests for bonding were performed using simple test pieces. The first part used indium evaporated through a shadow mask onto a piece of silicon. The second part had Cr/Au (50Å/500Å; chrome was deposited first) deposited uniformly onto a glass cover slip. The parts were cleaved, assembled face-to-face by hand, and placed into an annealing furnace. The alloying of the In into the Au could be observed during the anneal by looking through the back surface of the glass. After a few tries, it was observed that the pieces needed to be gently pressed together to obtain intimate metal-to-metal contact on all of the bond pads before the anneal started, because the parts would not collapse together on their own. Imperfections in the indium due to handling of the parts gave only small areas of metal to metal contact, but during the annealing process, these areas grew to the full size of the indium dots. The experiment showed that if a compression (or thermocompression) bond could be done, and if initial contact could be assured, then the parts could be reflowed in a furnace under a controlled atmosphere. The use of thin solder placed such strict requirements on the coplanarity of the parts that the flip chip aligner could not guarantee this perfect initial contact. Thus, for the real devices, a constant, but small,

applied pressure would be used to bring the samples closer and together as the solder layer melted and flowed. The next step was to create a process for the flip chip bonder using these test samples.

Flip chip bonder

To obtain the necessary positioning accuracy, pitch and roll resolution, and control of the bonding forces necessary for this project and their own VOI project, a commercial flip chip bonder was purchased by the Photonics Center (OCPA) at Rome Laboratory. The model M8-A Flip Chip Aligner/Bonder from Research Devices[59] was used for all of the bonds in this dissertation. This machine uses a beamsplitter and upward- and downward-looking cameras to position the wafers in X and Y and pitch and roll. The upper and lower chuck temperatures are independently controllable up to 400° C and the bonding force is monitored by a strain gauge and automatically regulated to a user-defined setpoint.

The manufacturer specifies a ±2 μm X and Y positioning accuracy, and it was found that this accuracy can be realized. Although the parts were typically bonded with a slight pitch and roll error, z-dimension accuracies of ±1-3 μm over a 2 mm long part were achieved, as indicated by the fact that most of the devices were contacted when using between 1 and 2 μm of solder. If it had been possible to use thicker solder, then the very accurate X and Y placement of the machine would make it a perfect thermocompression bonder, after which the tacked samples could be reflown either on the lower chuck without any applied pressure, or in an inert or reducing atmosphere in a furnace.

To determine a bonding process, the same In on Si and Cr/Au on glass samples were used. Bonding cycles with different temperatures and hold times were tried until it was found that a large amount of force was required to separate the two parts. For the best samples, the Si wafer would chip away in places before the bond failed.

In the accepted recipe, before bringing the parts together, the VCSEL (top chuck) was heated above the indium melting point while maintaining the sink (lower chuck) near room temperature. Keeping the lower chuck cool minimized the Au-In interactions on the sink while the bonding sequence was initiated. After contact, the samples were ramped up to 250°C in a few steps and held there for 3-5 minutes. This hold time is longer than necessary, but was thought to help take

the bond to completion for the pads where little metal to metal contact occurred. The amount of force applied during a bond is critical to device performance. A pressure of 4500 psi has been found to produce reliable devices, while 6000 psi had been seen to damage devices[60]. For each die to be bonded, the amount of contact area was determined and an appropriate pressure was programmed into the machine. Typical forces were 250 to 450 grams and typical times and temperatures for the upper and lower chucks are shown in Figure 5.10. A linear array (2×8 devices) of VCSELs bonded to a GES diamond heat sink is shown in Figure 5.11.

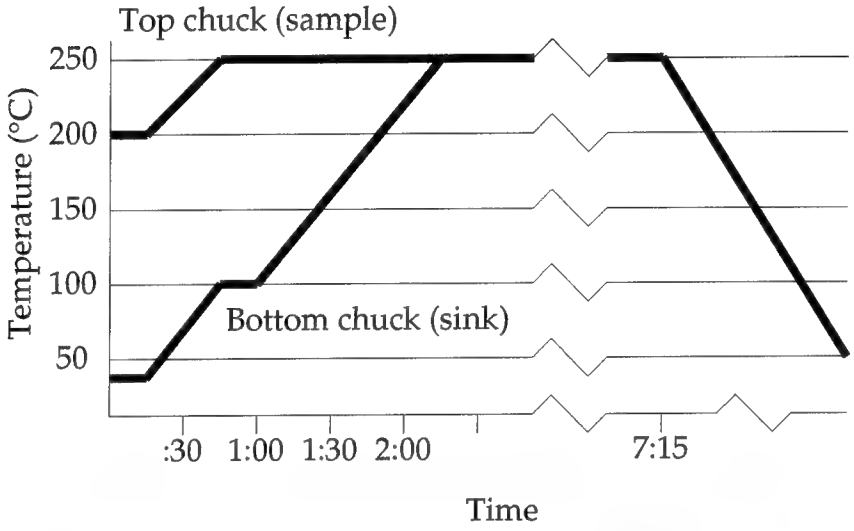

Figure 5.10: Temperature cycles of the bonding recipe

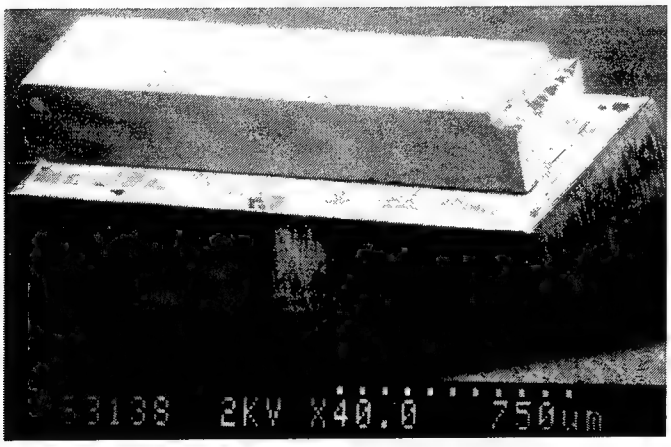

Figure 5.11: Linear VCSEL array bonded to diamond

Thermal Analysis of a VCSEL

One question that arose during the development of the flip chip process was whether or not this would make a difference. Thus a simple, analytic thermal analysis of a VCSEL was performed. REFLECT was modified so that the same input file structure could be used for the thermal analysis as was used for the reflectivity analysis. The resulting .TFILE was used as input to a modified REFLECT subroutine that calculated the thermal resistance of each layer and added a term, $2\pi hR/\{h-R\}$, where h is the substrate thickness and R is the radius of the VCSEL, for the thermal spreading resistance of a disk on a thick substrate.

The results were that the thermal resistance was very insensitive to the substrate thickness, but extremely sensitive to the VCSEL diameter as shown in Figure 5.12. The VCSELs in this work are etched only about three Bragg pairs past the active region, so thermal resistance values for 1-layer, 3-layers, and 20 layers have been calculated. The 3-layer calculation is for a junction-up configuration where the heat generated in the active region has to pass through only 3 layers before it can start spreading in the substrate. The 20-layer case is for the flip chip device, where the heat has to go through the entire upper mirror before getting to the heat sink.

Diameter	5 (μm)	10	15	20	25	30	60
1-pair resistance	349°C/W	87.4	38.8	21.8	14.0	9.71	2.43
3-pair resistance	1047	262.2	116.4	65.4	42.0	29.1	7.3
20-pair resistance	6980	1748	776	436	280	194	48.6
100μm substrate	1410	687	446	326	253	205	84.4
300μm substrate	1440	714	473	353	280	232	112

Figure 5.12: Thermal resistance of VCSELs (thermal resistance in °C/W)

These calculations made several assumptions. They assumed that the VCSEL was a straight-walled cylinder instead the actual tapered mesa so the thermal resistance is overestimated for the small diameter devices by a large amount. For example, the 5 μm diameter VCSEL actually has about a 13 μm diameter base and thus its thermal resistance is closer to 200°C/W than 1047°C/W. The calculations also ignored the difference in thermal resistivity of the first few microns of the substrate in the calculation of thermal resistance of the substrate. The formula that was used for the thermal resistance of the substrate is a semi-infinite approximation, so by using the numbers in the table for larger devices, the initial substrate spreading resistance can be estimated (noting that one Bragg pair is approximately 1600Å thick) and added to the thermal resistance of the substrate.

Using the above guidelines, the calculations predict that devices larger than about 15 μm in diameter will behave better in the flip chip configuration than in the junction up configuration. For smaller devices, the small mesa is just too thermally resistive for the flip chip configuration. If the wet-dry process is to be used, then the break-even point for efficient heat removal in the junction-down configuration will move to smaller devices.

Indium was chosen as the flip chip bonding solder because of its availability, ease of evaporation, and the fact that it readily alloys with gold. Thin solders (1-2 μm) were used in this project because the bonds were made directly on top of the VCSEL mesas and solder dams were not employed. No self-alignment was observed or expected with these thin solders, but good alignment accuracy (better than ±3 μm in X and Y) was provided by a high quality flip chip bonder, and high-yield bonds were produced. Au/In alloying during the solder evaporation raised the required reflow temperature to 250° C (instead of the 157° C melting point of the indium), but initial studies with a chrome diffusion barrier look promising for reducing the initial Au/In intermixing and for reducing the reflow temperature.

6. VCSEL CHARACTERIZATION

The characterization of the performance of the VCSELs was driven by the requirements of the VOI project and interest in the high speed performance of the devices. For the VOI project, the devices did not have to be state of the art, but did have to greatly outperform the LEDs currently in use in terms of output power. The VCSELs also had to operate CW so that microwave measurements could be performed on them. For both projects, they had to be flip chip bonded without damaging the devices. The LEDs currently used in the project emit ~10 μW into the half-plane above the device, while the 15μm diameter VCSELs emitted 100s of μW of light into a multi-mode fiber and larger devices produced several mW of pulsed optical power. Devices varying in size from 10 μm diameter to 30 μm diameter operated CW and devices were packaged with little or no damage and performed well under microwave modulation.

Unbonded device

The results presented in the next subsections describe the PI, PIV, and spectral measurements of different size VCSELs from two different wafers. In general, the two wafers behaved very similarly. The first wafer had a near-threshold emission wavelength of about 0.998 μm while the second emitted at about 1.016 μm near threshold. The thresholds on small devices from the second wafer were a couple mA higher than on the first. This difference was most likely due to a larger offset between the quantum well emission wavelength and the optical cavity length. Thus, slightly more heating was necessary to attain the threshold condition.

PI, PIV, and spectral measurements

The devices were directly probed with coplanar waveguide probes and the pulsed or CW current was supplied by an ILX Lightwave LDP 3811. A pulse length of one microsecond was used for all constant duty cycle measurements. Power measurements were either made with a broad area germanium photodetector or with a fiber-coupled germanium photo–detector. Fiber coupling efficiency into a 62.5 μm diameter core fiber optic cable was between 30 and 60%. Spectral measurements were obtained from a fiber-coupled optical spectrum analyzer.

The PI curves as a function of duty cycle for a 20μm diameter device are shown in Figure 6.1. Figure 6.1a shows the raw time-averaged power curves, while in Figure 6.1b the pulsed curves have been scaled by 1/(duty cycle). The reduction in device efficiency with an increase in duty cycle is consistent with the effects of an increase in junction temperature. This rise in junction temperature results in both (1) detuning of the gain spectrum and the cavity wavelength, and (2) an increased spread in the electron and hole distributions which reduces the gain. Similar reductions in the output power were observed as the pulse length was increased to 10s or 100s of microseconds.

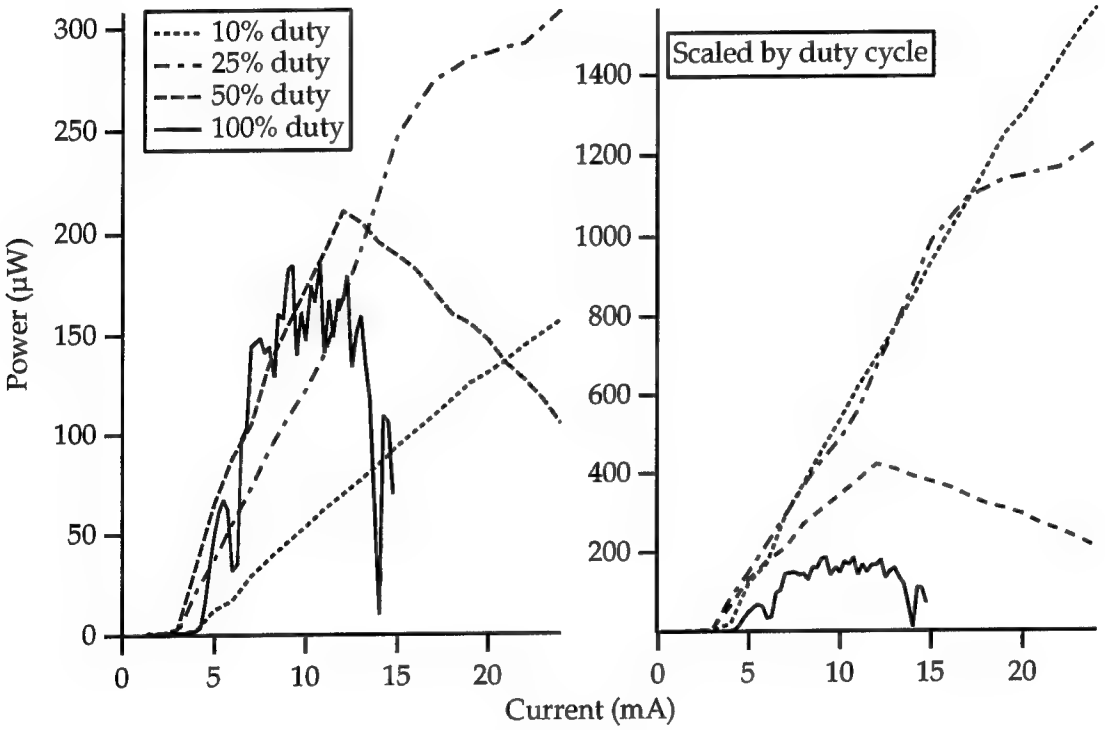

Figure 6.1: PI curves as a function of duty cycle

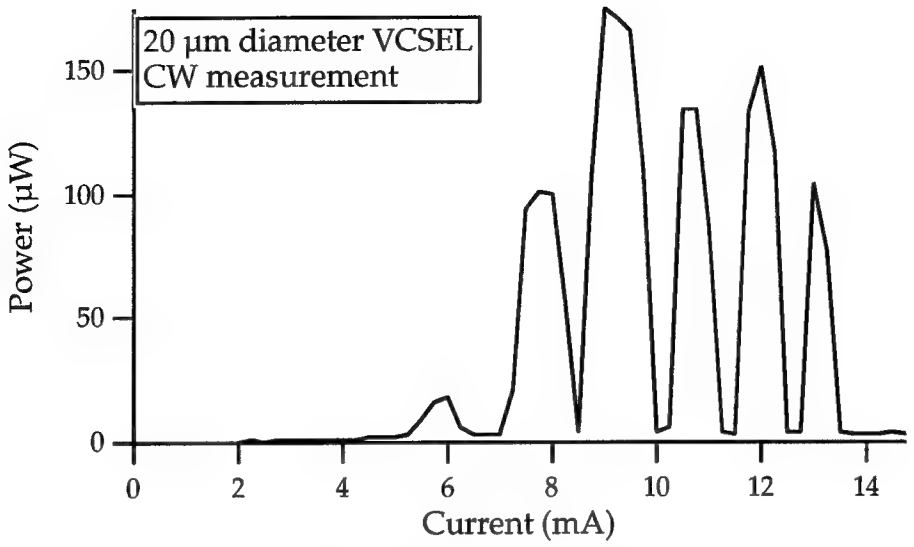

Figure 6.2: CW PI measurement

The CW measurement in Figure 6.1 is very jagged. When more datapoints were taken, as shown in Figure 6.2, an interesting effect was observed. There are ranges of current in which the lasing mode is extinguished. This effect was due to the external cavity that is formed between the bottom mirror and the polished back surface of the wafer. The reflection couples ~30% of the lasing mode back into the cavity, which, when out of phase with the laser mode, quenches the laser action. This effect repeats many times during a PI curve because the wavelength red-shifts with the increased heating at higher bias currents. This small change in wavelengths was enough to shift between the cavity modes of the substrate[61]. Using the refractive index of GaAs at a wavelength of 1 μm, and the measured difference in emission wavelengths at the maximums in output power, a cavity length of 300 μm was calculated, which was very close to the measured thickness of the substrate. An anti-reflection (AR) coating layer would solve, or at least reduce, this problem. The refractive index of SiO (~1.87) is very close to the geometric mean of the refractive indices of GaAs and air, so if its refractive index and thickness could be accurately controlled, SiO would make an exact 1-layer index-matching AR coating.

As mentioned in the section on processing, there was a very significant problem with current spreading in these devices. The cross-section of a 10 μm diameter device is shown in Figure 6.3. The 10 μm diameter contact sits on top of an 11-12 μm diameter mesa that was ~4 μm high. Thus, the base of the mesa was 18-19 μm in diameter while only the area under the metal mirror is truly considered active area. For large devices, the loss of drive current is a small percentage

change, but for small devices, the large width of the base region relative to the mesa contact area resulted in a reduction of current density at the active region by at least a factor of 2:1.

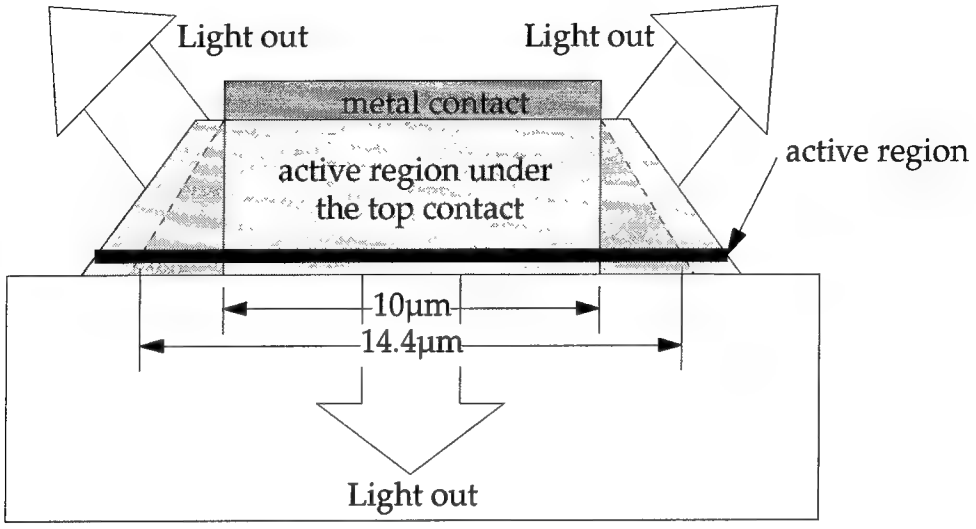

Figure 6.3: Cross-section of a 10 μm diameter device

The threshold current for several sizes of devices on the first wafer were compared and the current densities were calculated. Figure 6.4 shows the threshold current densities for devices on the first wafer as well as corrected curves which use the contact pad diameter plus 4 μm and plus 8 μm for determining the cross-sectional area of the device. (The solid lines are only to guide the eye.) Although it was not quantified, current spreading beyond the contact was significant as strong emission from these regions was observed on all lasers and LEDs that were tested.

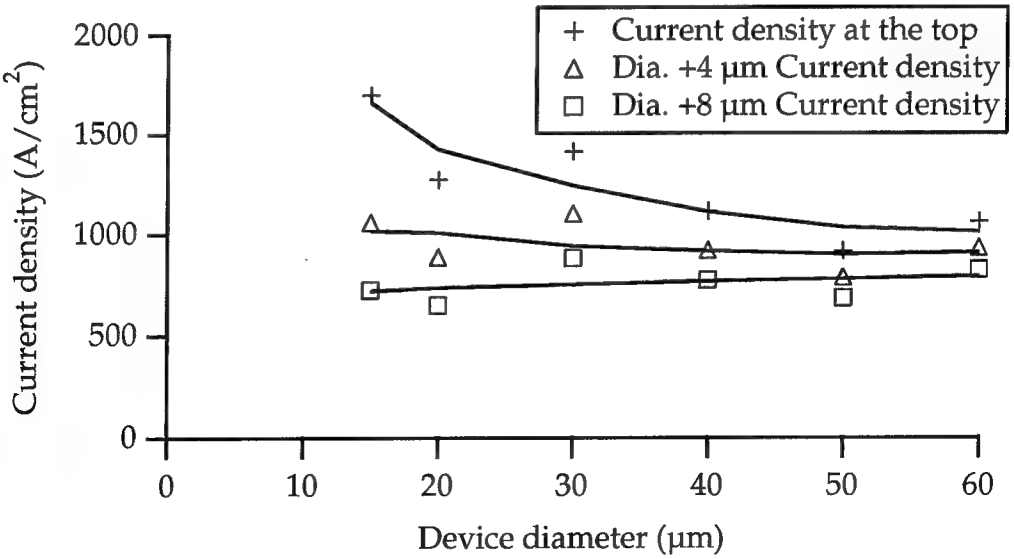

Figure 6.4: J_{th} and $J_{th\_effective}$ on the first wafer

PIV measurements

For the pulsed PIV measurements, the devices were probed as before, but two channels of a boxcar averager were used to measure the voltage before and after the diode. The high input impedance of the channels were assumed to not affect the amount of current reaching the laser and no special current monitoring was employed.

The results of a PIV measurement on a 15 μm diameter VCSEL from the first wafer is shown in Figure 6.5. At maximum power out, this and most other devices showed a wall plug efficiency of 1.0 to 1.5%. This low efficiency is due to the large voltage drop across the p-type mirror, the small amount of light which actually does escape the cavity through the 20-pair Bragg mirrors, and the loss of current density due to current spreading in the mesas.

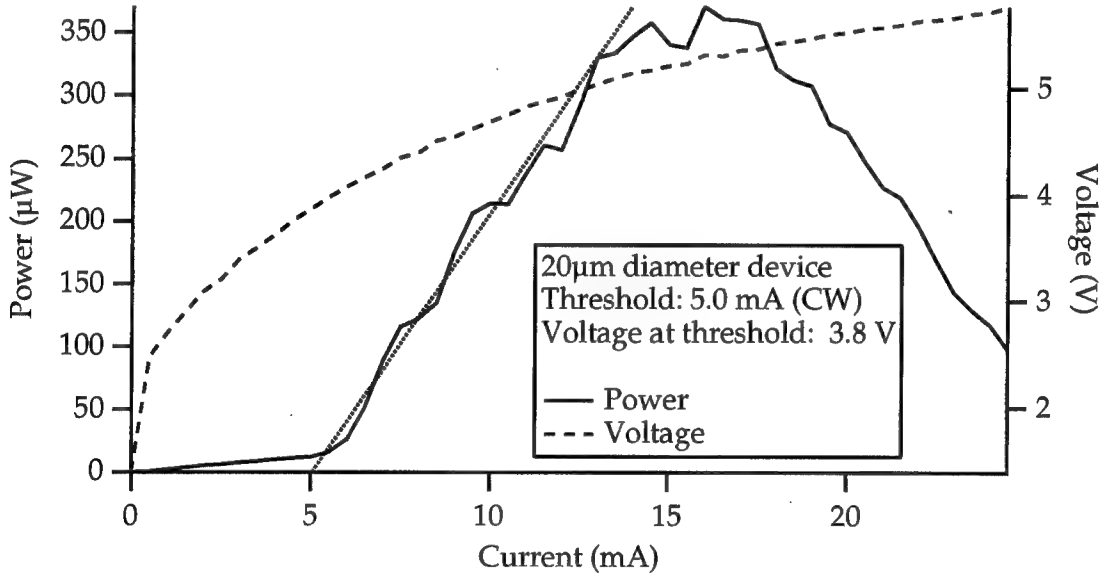

Figure 6.5: PIV measurement on a 15 μm diameter VCSEL

By observing the shift in emission wavelength as a function of input current and power, the increase in junction temperature was determined. A shift in junction temperature is expected, and, if the device is designed correctly, can result in device operation over extended current ranges[62]. The excessive losses in the device that resulted in a low wall plug efficiency also caused the cavity temperature to rise too quickly. Thus, the designed small offset between the

gain spectrum and the cavity wavelength (10 nm) was too small and the device only operated over a very limited range of currents. For a 15 μm diameter VCSEL from the second wafer (threshold = 4.6 mA), the change in wavelength was measured as a function of input current and voltage (and thus power), and is shown in Figure 6.6. The highest output power occurred at 8 mA which showed a $\Delta\lambda$ of 3.4 nm which corresponds to a ΔT of ~40° C[62] at an input power of 30 mW. The device emission returns to the nW level at a drive current of ~18 mA at which point the ΔT is near 110° C. The 1.13Å / mW change in emission wavelength is only slightly higher than previously reported[62].

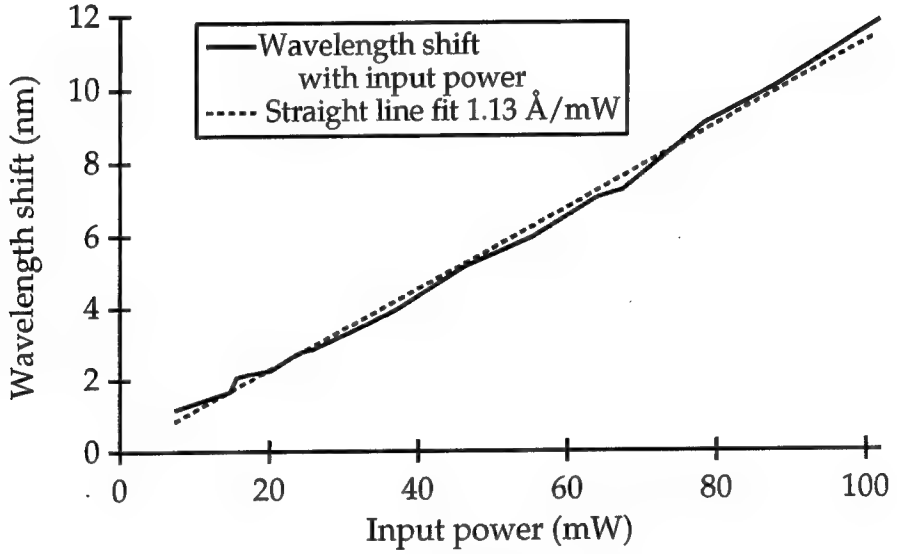

Figure 6.6: Shift in emission wavelength with input power

Emission Spectrum

The small devices (< 30μm diameter) showed single mode output for almost all bias currents while larger devices were multi-mode for much of their operating range. Excellent side mode suppression ratio (> 50 dB) is shown in Figure 6.7 for a 20 μm diameter VCSEL. This spectrum was taken at a peak in a CW spectrum, but spectra taken at the nulls also showed similar single mode behavior at a much lower power levels.

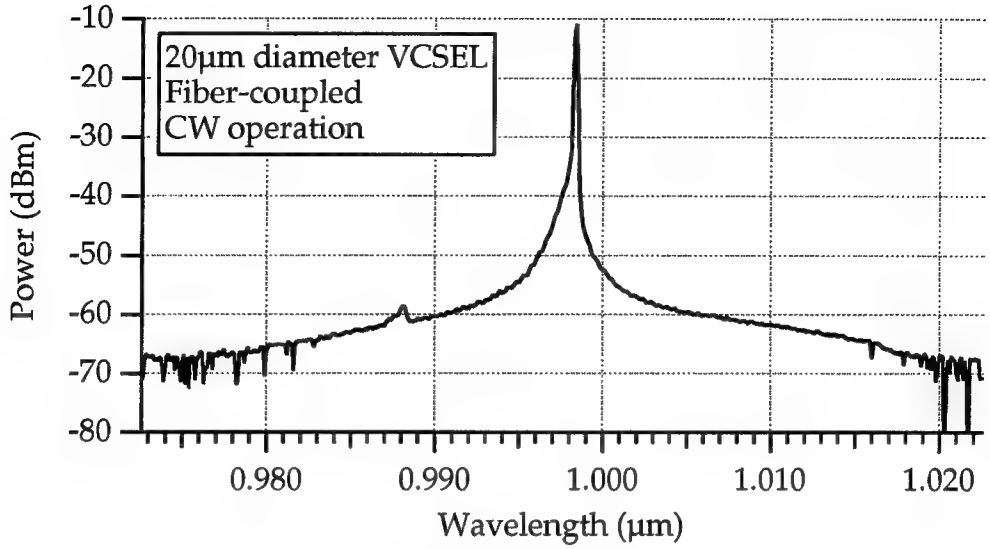

Figure 6.7: Emission spectrum

Bonded devices and microwave results

The first set of VCSELs to be bonded was a 4×4 array of 10 μm diameter devices. They were bonded to a sapphire heat sink using 2 μm of indium solder. While sapphire is a good thermal conductor at low temperatures (77 K or below), its room temperature thermal conductivity is below that of GaAs. Thus, the sapphire was used more as an insulating carrier than as a heat sink. Several of the CPW feeds to the devices were probed and most devices lased, with threshold currents between 3 and 4 mA. The 10 μm diameter devices were too small to be probed with the CPW probes, but based on the results from 15 and 20 μm diameter devices, thresholds of ~3 mA on 10 μm diameter devices were expected. The similarity in thresholds before and after bonding shows that the bonding technique is a very low damage process.

To measure the microwave characteristics of these packaged devices, a test station was assembled. The laser was modulated using the signal from a vector network analyzer (VNA) while the DC component of the signal was supplied by a CW current source attached to a bias tee on port 1 of the VNA. The laser emission was collimated using a 0.23 pitch graded index (0.23P GRIN) rod and then focused into a single mode fiber (SMF) pigtailed to a 0.25P GRIN rod. All GRIN rods used were designed for 1300 nm light, but worked adequately for collecting ~1 μm light. The SMF was attached to a high speed photodetector and the received microwave signal was directed to port 2 of the VNA. This setup is shown in Figure 6.8.

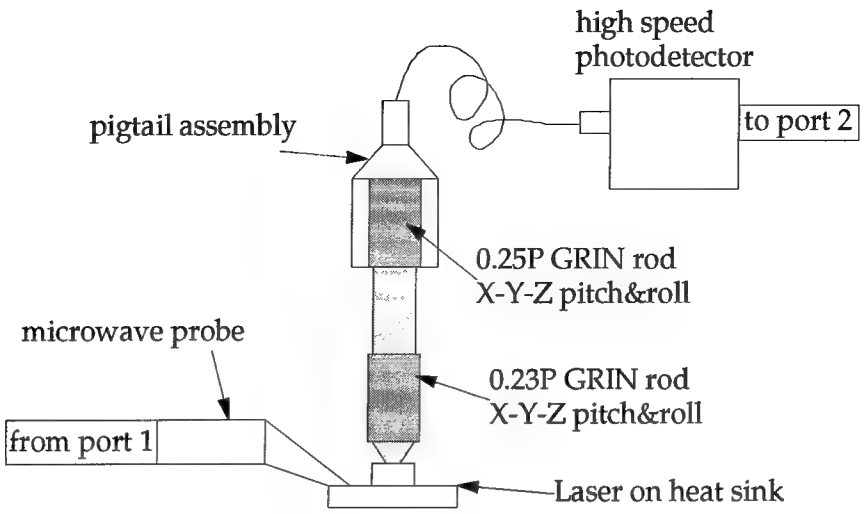

Figure 6.8: Beam focusing setup

Launching into the SMF was necessary because the coupling onto the 25 μm diameter detector is optimized for an 8 μm core SMF. The alignment sequence started with simple X-Y-Z positioning of the 0.23P GRIN rod, using an IR card to view the focused beam. The collection of light into the SMF was made easier by first doing the alignment with a multi-mode fiber (MMF) pigtailed to a 0.25P GRIN rod. After this first coarse alignment, the MMF assembly was removed and replaced with the single mode assembly. This sequence always resulted in a relatively large signal coupled into the SMF with only small variations in pitch and roll and X-Y-Z needed to optimize the coupling.

The highest measured bandwidth for the devices bonded to sapphire was ~3.7 GHz for a 10 μm diameter device at a drive current of 6.5 mA. The goal of bonding devices to diamond was to see a difference in device performance, both in a higher threshold (showing better heat sinking) and in a larger modulation bandwidth.

The devices bonded to diamond did show signs of being heat sunk. Devices of 10 and 15 μm diameter were bonded to GES diamonds with 1 μm of indium solder using the same recipe as used for the devices bonded to sapphire. The 10 μm diameter devices showed thresholds greater than those devices bonded to sapphire and the 15 μm diameter devices showed thresholds higher than unbonded devices. The threshold lasing wavelengths of these devices were almost identical to each other and to those of the unbonded devices. This agreement indicated that the bonding process, again, had not damaged the devices. However, that fact that more drive current was

necessary to sufficiently warm the devices so that the gain spectrum could overlap the cavity wavelength shows that the offset between gain and cavity is too large for low-current (<5 mA) operation of the bonded devices. The maximum -3dB bandwidth measured was 6.6 GHz and was obtained on a 15μm diameter device at a drive current of 9.3 mA, as shown in Figure 6.9.

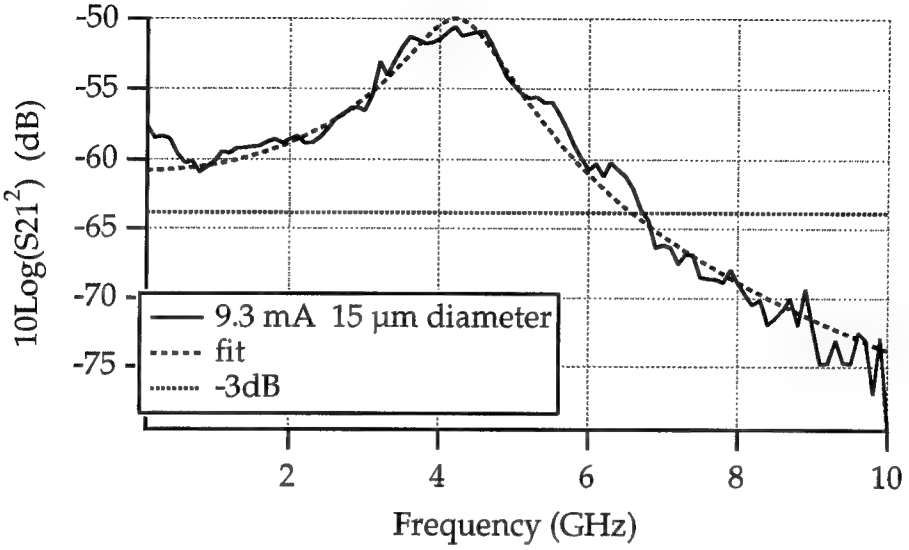

Figure 6.9: 6.6 GHz -3dB modulation bandwidth of a bonded VCSEL

The fabricated devices showed room temperature continuous wave operation and emitted light in a single mode. Because of the high mirror reflectivity, output powers were a modest 200 - 500 μW under CW conditions, and only a few mW under short-pulse, high-current operation. Equally important, the mirror stacks also caused a large amount of resistive heating of the devices. The interesting on-off behavior of the PI curves is easily understood by analyzing the modes of the cavity formed by the bottom mirror stack and the polished back surface of the substrate, and can be greatly reduced by a bottom-surface AR coating.

The microwave performance of the devices, although not a new record, is impressive, considering the number of potentially performance-degrading device properties. This result, and good CW PI curves from edge-emitting lasers made out of the same material, show that an active region of highly-strained In_3Ga_7As quantum wells is a good one, and offers the potential for higher speed VCSELs in the future.

Future work with the VCSELs should address the high turn-on voltages. Parabolic instead of sinusoidal grading can be tried, but, the difference in Al mole fraction between the two grading schemes is very small. Little improvement is expected. Heavier doping in the low light intensity grades will probably make the most difference. The mirror stacks can each be reduced by two pairs in order to reduce the turn-on voltage (p-type) and to increase the output powers (n-type). With the different thermal load of bonded devices, the offset between the gain spectrum and cavity mode should remain small, but the thermal sinking of the device and junction temperature as a function of bias current needs to be investigated further before designing the next wafers. The wet-dry process should also be investigated further to eliminate the loss in current density that was observed in the wet chemically etched VCSELs. Other processing techniques such as intracavity contacts and oxidation of the exposed AlGaAs could also be investigated.

In the bonding process, more solder could be used to help alleviate some of the pitch and roll problems and possibly allow for a reflow in a controlled atmosphere furnace. Indium will wet almost any material so the top of the Au layer on both the contacts could have a diffusion barrier (Pd, Pt, W, Cr) added to it. If oxidation of the diffusion barrier is a concern, then a 100-200 Å flash of gold could be used to protect it. This diffusion barrier would eliminate or at least reduce the In-Au alloying and would allow the bonds to take place at a much lower temperature. With 3-5 μm of solder, a collapse effect might be observed and reflow at lower temperatures without any applied pressure could be used. This method of bonding would eliminate any crystal damage to the small device mesas. 10-20 μm of solder would result in better self-alignment and self-planarization, but the low thermal conductivity of indium and the requirements of solder dams and thick solder evaporations might not make that approach practical.

"Vertical Cavity Surface Emitting Lasers for Flip-Chip Packaged Vertical Optical Interconnects", S.S. O'Keefe, W.J. Schaff, and L.F. Eastman, *Spie's Int. Symp on Optical Engineering in Aerospace Sensing* - Conference **2216** Photonics at the Air Force Photonics Center, Orland, Fl, April 4-5, 1994 Proc 181-188

"CPW Transmission Lines on Polycrystalline Diamond Substrates for a 4x4 VCSEL Array", S.S. O'Keefe, G. Martin, D.W. Woodard, W.J. Schaff and L.F. Eastman, *WOCSDICE'94* Cork, Ireland (May 29-June 2, 1994).

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REFERENCES

[1] A.Y. Cho, "GaAs epitaxy by a molecular beam method: observation of surface structure on the (001) face," *J. Appl. Phys.*, v. 42, no. 5, pp. 2074-2081, 1971.

[2] J.H. Neave, P.J. Dobson, B.A. Joyce, and J. Zhang, "Reflection high-energy electron diffraction oscillations from vicinal surfaces—a new approach to surface diffusion measurements," *J. Appl. Phys.*, v. 47, n. 2, pp. 100-102, 1985.

[3] J.H. Neave, B.A. Joyce, P.J. Dobson, and N. Norton, "Dynamics of film growth of GaAs by MBE from Rheed observations," *Appl. Phys. A.*, v. 31, pp. 1-8, 1983.

[4] P. Mandeville, "Molecular-beam epitaxial growth and characterization of pseudomorphic double-doped field effect transistor structures on gallium arsenide," (Ph.D. diss., Cornell University, 1993), pp. 22-25.

[5] J. Ralston, G.W. Wicks, and L.F. Eastman, "Reflection high-energy electron diffraction intensity oscillation study of Ga desorption from molecular bem epitaxially grown $Al_xGa_{1-x}As$," *J. Vac. Sci. Technol. B*, v. 4, n. 2, pp. 594-597, 1986.

[6] E.M. Gibson, C.T. Foxon, J. Zhang, and B.A. Joyce, "Gallium desorption from GaAs and (Al,Ga)As during molecular beam epitaxy growth at high temperatures," *Appl. Phys. Lett.*, v. 57, n. 12, pp. 1203-1205, 1990.

[7] P. Mandeville, S.S. O'Keefe, Y-P. Chen, J. Burm, unpublished, 1991.

[8] S.D. Offsey, W.J. Schaff, L.F. Lester, L.F. Eastman, and S.K. McKernan, "Strained-layer InGaAs-GaAs-AlGaAs lasers grown by molecular beam epitaxy for high-speed modulation," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1455-1461, 1991.

[9] R.S. Geels, B.J. Thibeault, S.W. Corzine, J.W. Scott, and L.A. Coldren, "Design and Characterization of $In_{0.2}Ga_{0.8}As$ MQW vertical-cavity surface-emitting lasers," *IEEE J. Of Quantum Electron.*, v. 29, n. 12, pp. 2977-2987, 1993.

[10] R.S. Geels, S.W. Corzine, and L.A. Coldren, "InGaAs vertical-cavity surface-emitting lasers," *IEEE J. Of Quantum Electron.*, v. 27, n. 6, pp. 1359-1367, 1991.

[11] J.L. Jewell, J.P. Harbison, A. Scherer, Y.H. Lee, and L.T. Florez, "Vertical- cavity surface-emitting lasers: design, growth, fabrication, and characterization," *IEEE J. Of Quantum Electron.*, v. 27, n. 6, pp. 1332-1346, 1991.

[12] R.S. Geels, S.W. Corzine, J.W. Scott, D.B. Young, and L.A. Coldren, "Low threshold planarized vertical-cavity surface-emitting lasers," *IEEE Photon. Technol. Lett.*, v. 2, n. 4, pp. 234-236, 1990.

[13] R.S. Geels, S.W. Corzine, and L.A. Coldren, "InGaAs vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1359-1367, 1991.

[14] J.L. Jewell, J.P. Harbison, A. Scherer, Y.H. Lee, and L.T. Florez, "Vertical-cavity surface-emitting lasers: design, growth, fabrication, characterization," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1332-1346, 1991.

[15] T.J. Rogers, C. Lei, D.G. Deppe, and B.G. Streetman, "Low threshold voltage continuous wave vertical-cavity surface-emitting lasers," *Appl. Phys. Lett.*, v. 62, n. 17, pp. 2027-2029, 1993.

[16] J.M. Catchmark, R.A. Morgan, K. Kojima, R.E. Leibenguth, M.T. Asom, G.D. Guth, M.W. Focht, L.C. Luther, G.P. Przybylek, T. Mullally, and D.N. Christdoulides, "Extended temperature and wavelength performance of vertical cavity top surface emitting lasers," *Appl. Phys. Lett.*, v. 63, n. 23, pp. 3122-3124, 1993.

[17] D.B. Young, J.W. Scott, F.H. Peters, B.J. Thibeault, S.W. Corzine, M.G. Peters, S.-L. Lee, and L.A. Coldren, "High-power temperature-insensitive gain-offset InGaAs/GaAs vertical-cavity surface-emitting lasers," *IEEE Phot. Tech. Lett.*, v. 5, n. 2, pp. 129-132, 1993.

[18] J.W. Matthews, and A.E. Blakeslee, "Defects in epitaxial multilayers," *J. Crystal Growth*, v. 27, pp. 118-125, 1974.

[19] D.Teng, P. Mandeville, and L.F. Eastman, "Growth limitation of strained multiple quantum wells," *J. Crystal Growth*, v. 135, pp. 36-40, 1994.

[20] D. Vakhshoori, J.D. Wynn, G.J. Zydzik, R.E. Leibenguth, M.T. Asom, and R.A. Morgan, "Top-surface emitting lasers with 1.9 V threshold voltage and the effect of spatial hole burning of their transverse mode operation and efficiencies," *Appl. Phys. Lett.*, v. 62, n. 13, pp. 1448-1450, 1993.

[21] P. Zhou, J. Cheng, C.F. Schaus, S.Z. Sun, K. Zheng, E. Armout, C. Hains, W. Hsin, D.R. Myers, and G.A. Vawter, "Low series resistance high-efficiency GaAs/AlGaAs vertical-cavity surface-emitting lasers with continuously graded mirrors grown by MOCVD," *IEEE Photon. Technol. Lett.*, v. 3, n. 7, pp. 591-593, 1991.
[22] S.A. Chalmers, K.L. Lear, and K.P. Kileen, "Low resistance wavelength-reproducible p-type (Al,Ga)As distributed Bragg reflectors grown by molecular beam epitaxy," *Appl. Phys. Lett.*, v. 62, n. 14, pp. 1585-1587, 1993.
[23] R.S. Geels, B.J. Thibeault, S.W. Corzine, J.W. Scott, and L.A. Coldren, "Design and characterization of $In_{0.2}Ga_{0.8}As$ MQW vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, v. 29, n. 12, pp. 2977-2987, 1993.
[24] K. Kojima, R.A. Morgan, T. Mullaly, G.D. Guth, M.W. Focht, R.E. Leibenguth, and M.T. Asom, "Reduction of p-doped mirror electrical resistance of GaAs/AlGaAs vertical-cavity surface-emitting lasers by delta doping," *Electron. Lett.*, v. 29, n. 20, pp. 1771-1772, 1993.
[25] M. Sugimoto, H. Kosaka, K.Kurihara, I. Ogura, T. Numai, and K. Kasahara, "Very low threshold current density in vertical-cavity surface-emitting laser diodes with periodically doped distributed Bragg reflectors," *Electron. Lett.*, v. 28, n. 4, pp. 385-387, 1992.
[26] M.G. Peters, B.J. Thibeault, D.B. Young, J.W. Scott, F.H. Peters, A.C. Gossard, and L.A. Coldren, "Band-gap engineered digital alloy interfaces for lower resistance vertical-cavity surface-emitting lasers," *Appl. Phys. Lett.*, v. 63, n. 25, pp. 3411-3413, 1993.
[27] C.E.C. Wood, "RED intensity oscillations during MBE of GaAs," *Surface Sci.*, v. 108, p. L441-L443, 1981.
[28] J.J. Harris, B.A. Joyce, and P.J. Dobson, "Oscillations in the surface structure of Sn-doped GaAs during growth by MBE," *Surface Sci.*, v. 103, p. L90-L96, 1981.
[29] P.J. Dobson, B.A. Joyce, J.H. Neave, and J. Zhang, "Current understanding and applications of the RHEED intensity oscillation technique," *J. Crystal Growth*, v. 81, pp. 1-8, 1987.
[30] OMS-1 Application note, "Fast determination of Growth Rates", Optical Solutions, Systems for epilayer characterization, P.O. Box 4517 Berkeley, CA 94704.
[31] J.L. Jewell, J.P. Harbison, A. Scherer, Y.H. Lee, and L.T. Florez, "Vertical-cavity surface-emitting lasers: design, growth, fabrication, characterization," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1332-1346, 1991.
[32] R.S. Geels, S.W. Corzine, and L.A. Coldren, "InGaAs vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1359-1367, 1991.
[33] S.D. Offsey, W.J. Schaff, L.F. Lester, L.F. Eastman, and S.K. McKernan, "Strained-layer InGaAs-GaAs-AlGaAs lasers grown by molecular beam epitaxy for high-speed modulation," *IEEE J. Quantum Electron.*, v. 27, n. 6, pp. 1455-1461, 1991.
[34] K. Knopp, National Institute of Standards and Technology, Electromagnetic Technology Division, Optical Electronic Metrology Group, 814.02, Optical Communication Device Metrology, 325 Broadway, Boulder, CO 80303-3328, (303)497-5342.
[35] Maj. G. Vansuch, Air Force Institute of Technology, Department of Engineering Physics, AFIT/EN-016, 2950 P Street, Building 640 Area B, Wright-Patterson AFB, OH 45433-7765, 513-255-3636, ext. 1489.
[36] Robert Spencer, private communication, 1995.
[37] Norton Diamond Film, Goddard Rd., Northboro, MA 01532-1545, 1-800-336-6115.
[38] GE Superabrasives, 6325 Huntley Rd., P.O. Box 568, Worthington, OH 43085, 1-614-438-2173
[39] Wafer Grip, by Dynatex Corp., 727 Shasta St., Redwood City, CA 94063.
[40] Zap-A-Gap, CA+, by Pacer Technology, 9420 Santa Anita Ave., Rancho Cucamonga, CA 91730, 714-987-0550.
[41] C.P. Wen, "Coplanar waveguide: a surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Trans. On Microwave Theory and Techniques*, v. MTT-17, pp. 1087-1090, 1969.
[42] K.C. Gupta, R. Garg, and I.J. Bahl, *Microstrip lines and slotlines*, (Dedham, Mass: Artech House, 1979), pp. 257-301.
[43] S.D. Offsey, W.J. Schaff, P.J. Tasker, and L.F. Eastman, "Optical and microwave performance of GaAs-AlGaAs and strained layer InGaAs-GaAs-AlGaAs graded index separate confinement heterostructure single quantum well lasers," *IEEE Photon. Tech. Lett.*, v. 2, n. 1, pp. 9-11, 1990.
[44] J. Braunstein, private communication, 1995.

[45] S.S. O'Keefe, G.H. Martin, D.W. Woodard, W.J. Schaff, and L.F. Eastman, "CPW transmission lines on polycrystalline diamond substrates for a 4 x 4 VCSEL array," *presented at the 1992 WOCSDICE*, Kinsale, Ireland, May 29 - June 1, 1994.
[46] L.F. Miller, "Controlled collapse reflow chip joining," *IBM J. Res. Develop.*, v. 13, n. 3, pp. 239-250,1969.
[47] W. Nakwaski, "An additional temperature increase within GaAs/(AlGa)As diode lasers caused by the deterioration of an indium solder," *Electron. Technol.*, v. 23, n. 1/4, pp. 33-38, 1990.
[48] V. Simic, and Z. Marinkovic, "Thin film interdiffusion of Au and In at room temperature," *Thin Solid Films*, v. 41, pp. 57-61, 1977.
[49] C.C. Lee, C.Y. Wang, and G. Matijasevic, "Au-In bonding below the eutectic temperature," *IEEE Trans. Comp. Hybrids, Manuf. Technol.*, v. 16, no. 3, pp. 311-316, May 1993.
[50] A. Katz, K-W. Wang, F.A. Baiocci, W.C. Dautremont-Smith, E. Lane, C-H. Lee, Y-M. Wong, K.L. Tai, D.D. Bacon, H.S. Luftman, and R.R. Varma, "Metallization systems for bonding of InP laser diodes to CVD-diamond submounts," *Proc. Of Mat. Res. Soc. Symp.*, v. 260, pp. 889-903, 1992.
[51] T.G. Finstad, T. Anderson, and T. Olsen, "Characterization of evaporated gold-indium films on semiconductors," *Thin Solid Films*, v. 29, pp. 145-154, 1975.
[52] M. Millares, B. Pieraggi, and E. Lelievre, "Multiphase reaction-diffusion in the Au-In system," *Scripta Metall.*, v. 27, pp. 1777-1782, 1992.
[53] K. Shimizu, T. Nakanishi, K. Karasawa, K. Hashimoto, and K. Niwa, "Solder joint reliability of indium-alloy interconnections," *J. Electron. Mater.*, v. 24, n. 1, pp. 39-45, 1995.
[54] C.H. Lee, K.L. Tai, D.D. Bacon, C. Doherty, A. Katz, Y.M. Wong, and E. Lane, "Bonding of InP laser diodes by Au-Sn solder and tungsten-based barrier metallization schemes," *Semicond. Sci. Technol.*, v. 9, pp. 379-386, 1994.
[55] G.S. Matijasevic, C.Y. Wang, and C.C. Lee, "Void free bonding of large silicon dice using gold-tin alloys," *IEEE Trans. Comp. Hybrids, Manuf. Technol.*, v. 13, n. 4, pp. 1128-1134, Dec. 1990.
[56] R.P. Elliott, ed., *Constitution of Binary Alloys, First Supplement*, (New York: McGraw Hill, 1965), pp. 72-73.
[57] J.M. Poate, K.N. Tu, and J.W. Mayer, ed., *Thin Films - interdiffusion and reactions*, (New York: John Wiley & Sons, 1978), pp. 342-344.
[58] C.D. Hodgman, ed., *Handbook of chemistry and physics, 43rd edition*, (Cleveland: The Chemical Rubber Publishing Co, 1961), p. 405-435.
[59] M8-A Flip Chip Aligner/Bonder, by Research Devices, 121 Ethel Rd. West, Piscataway, NJ, 08854.
[60] L.F. Eastman, private communication, 1995.
[61] C.J. Chang-Hasnain, J.P. Harbison, C. Zah, M.W. Maeda, L.T. Florez, N.G. Stoffel, and T-P. Lee, "Multible wavelength tunable surface-emitting laser arrays," *IEEE J. of Q. Electron.*, v. 27, n. 6, pp. 1368-1376, 1991.
[62] D.B. Young, J.W. Scott, F.H. Peters, B.J. Thibeault, S.W. Corzine, M.G. Peters, S.-L. Lee, and L.A. Coldren, "High power temperature-insensitive gain-offset InGaAs/GaAs vertical-cavity surface-emitting lasers," *IEEE Photon. Technol. Lett.*, v. 5, n. 2, pp. 129-132, 1993.

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